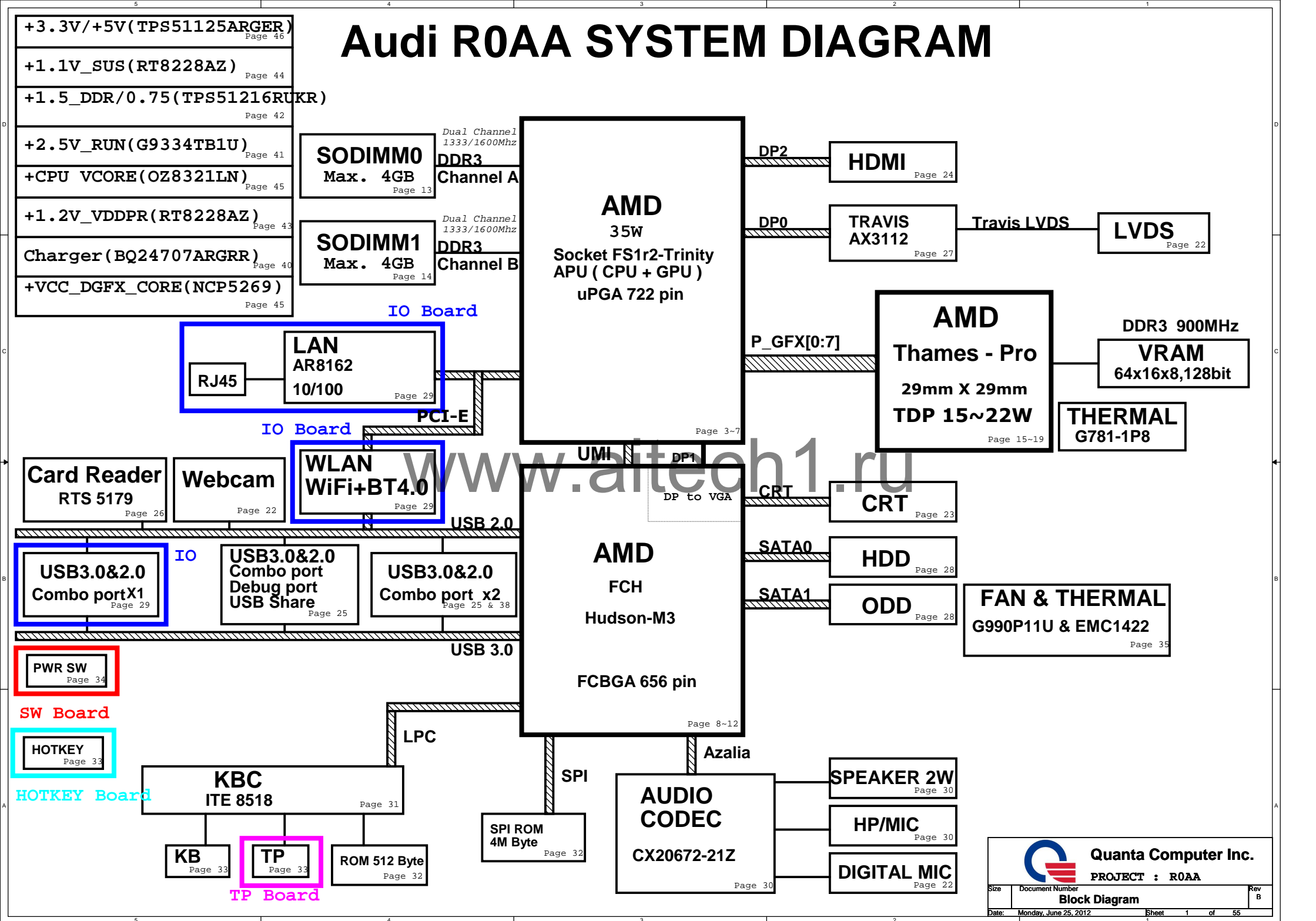


Audi ROAA SYSTEM DIAGRAM

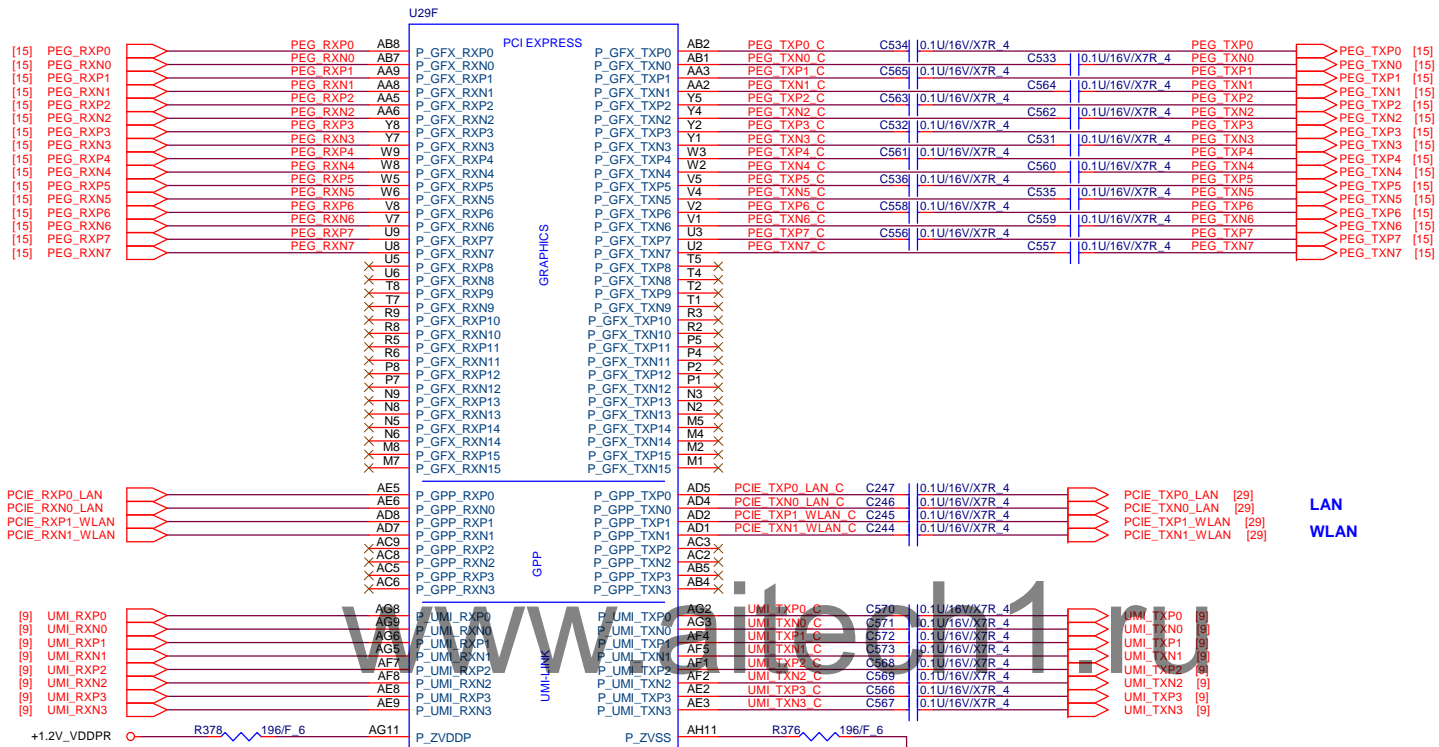


USB Master	Port Assignment
USB0	DEBUG
USB1	MiniCard 1 (WLAN/BT)
USB2	NC
USB3	NC
USB4	NC
USB5	NC
USB6	NC
USB7	Card Reader
USB8	NC
USB9	Camera
USB10	External port#1 (USB3.0)
USB11	External port#2 (USB3.0)
USB12	External port#3 (USB3.0)
USB13	External port#4 (Power share)

SATA Master	Port Assignment
SATA0	HDD
SATA1	ODD
SATA2	NC
SATA3	NC
SATA4	NC
SATA5	NC

PCIE Master	Port Assignment
CPU_GPP 0	LAN
CPU_GPP 1	WLAN
CPU_GPP 2	NC
CPU_GPP 3	NC
FCH_GPP 0	NC
FCH_GPP 1	NC
FCH_GPP 2	NC
FCH_GPP 3	NC

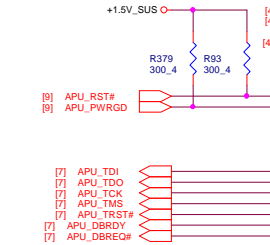
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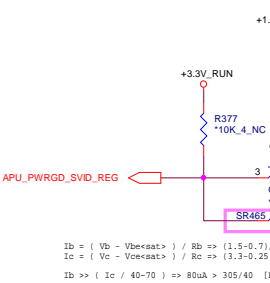
SVC_SVD		BOOT VOLTAGE	
VFX#02_VRM	= GND	VFX#02_VRM	= HIGH
0	0	1.1	1.4
0	1	1.0	1.2
1	0	0.9	1.0
1	1	0.8	0.8

+1.5V_SUS

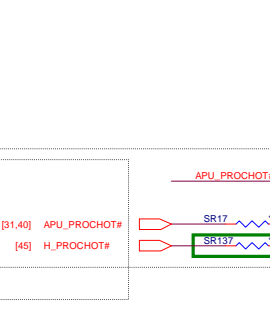
Note: CLK_APU_HCLKP/N is 100MHZ SSC
Note: CLK_DP_NSSCP/N is 100MHZ non-SSC



[45] APU_VDD_RUN_FB_L
[45] APU_VDDNB_RUN_FB_H
[45] APU_VDD_RUN_FB_H



$I_b = (V_b - V_{be(sat)}) / R_b \Rightarrow (1.5 - 0.7) / 10 = 80\mu A$
 $I_c = (V_c - V_{be(sat)}) / R_c \Rightarrow (3.3 - 0.25) / 10 = 305\mu A$
 $I_b \gg (I_c / 40 - 70) \Rightarrow 80\mu A > 305 / 40$ [BJT is on sat status]



[31,40] APU_PROCHOT#
[45] H_PROCHOT#

DP0 to LVDS

DP1 to FCH VGA

HDMI

Trinity APU

Debug only(Remove after MP)

100K R near APU

HDMI Hot-plug

CRT Hot-plug

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Quanta Computer Inc.

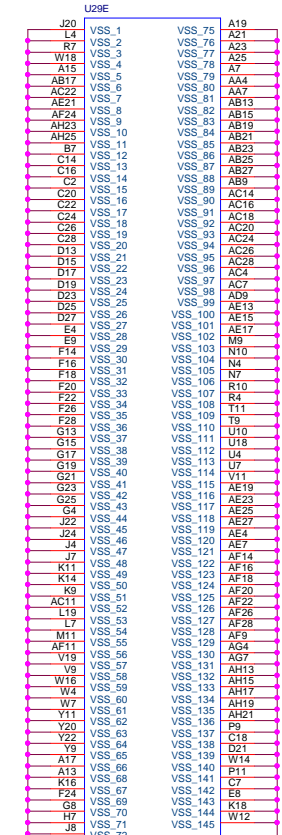
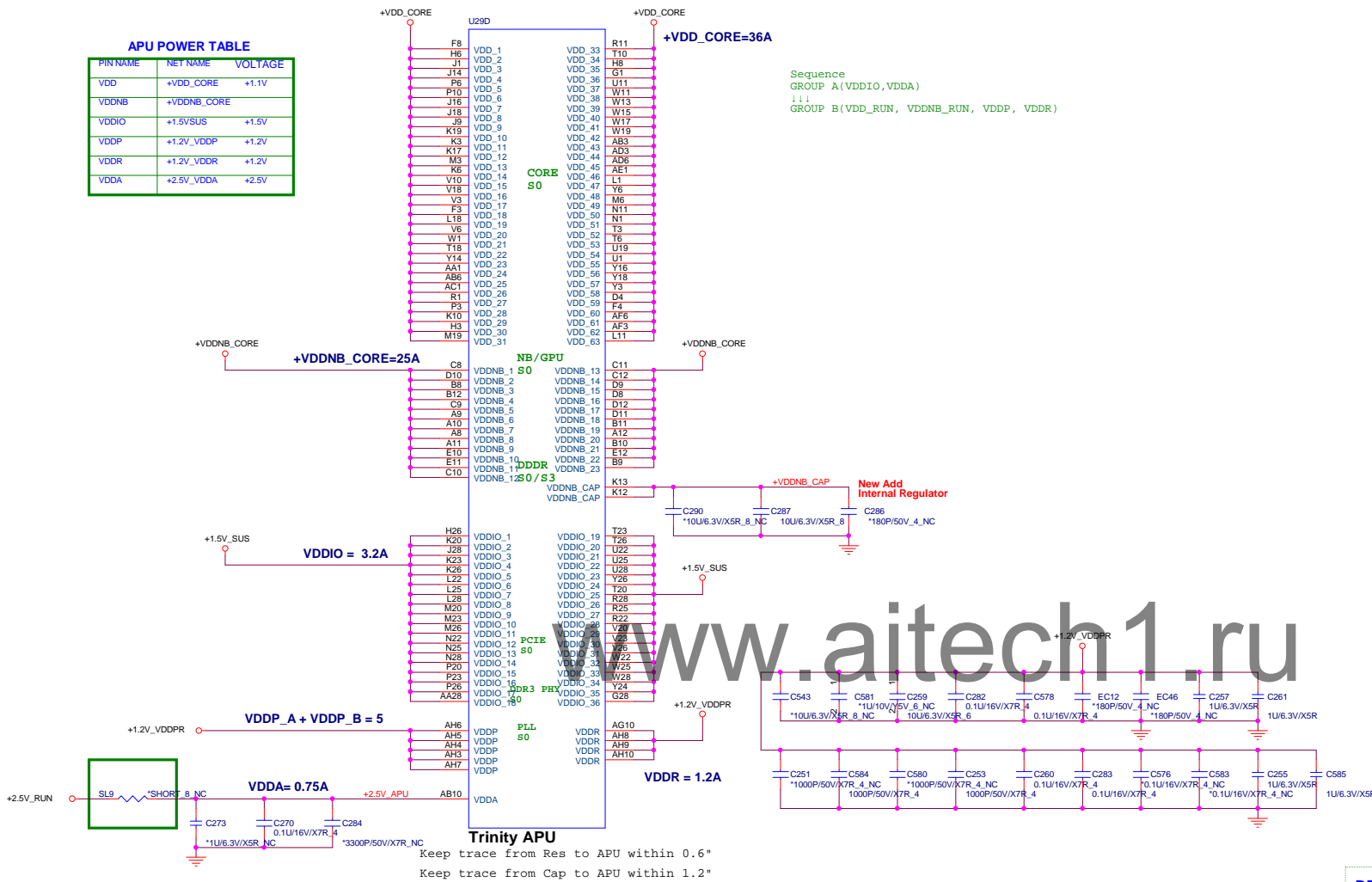
PROJECT : ROAA

Size Document Number Display/Misc Rev B

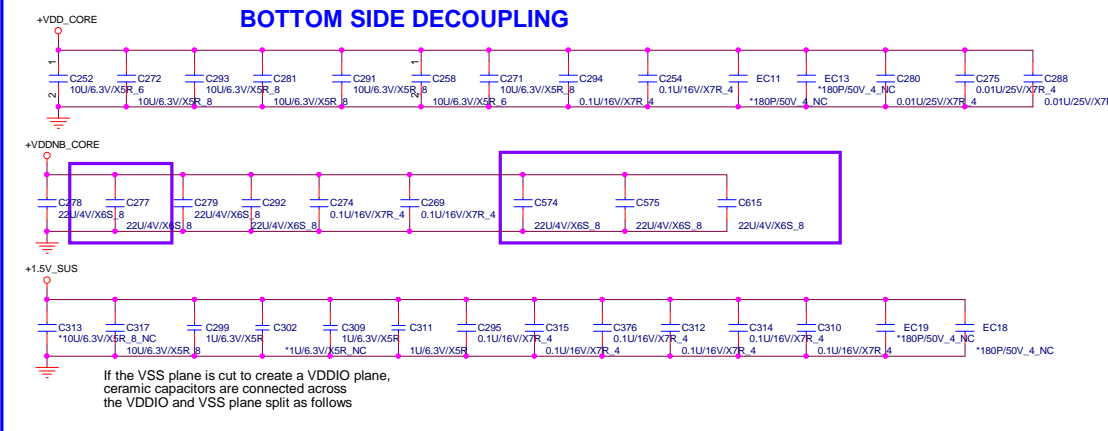
Date: Monday, June 25, 2012 Sheet 5 of 55

APU POWER TABLE

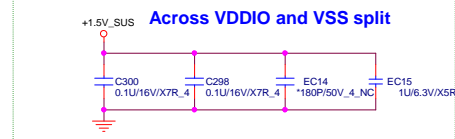
PIN NAME	NET NAME	VOLTAGE
VDD	+VDD_CORE	+1.1V
VDDNB	+VDDNB_CORE	
VDDIO	+1.5V_SUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V



BOTTOM SIDE DECOUPLING

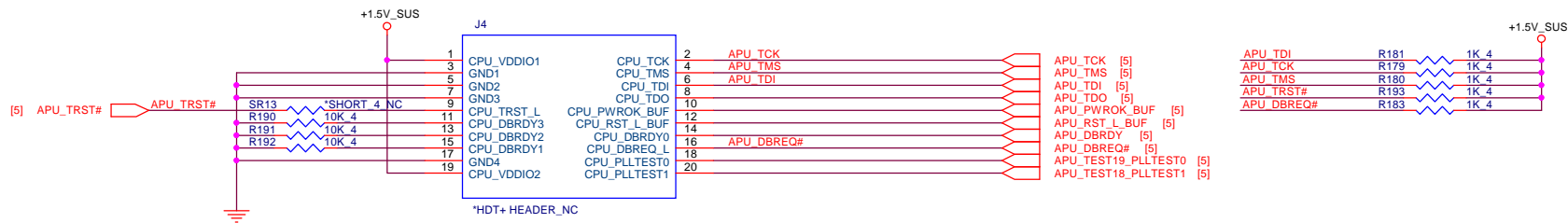


DECOUPLING between PROCESSOR and DIMMS



HDT+ Connector

Debug only
Remove after MP



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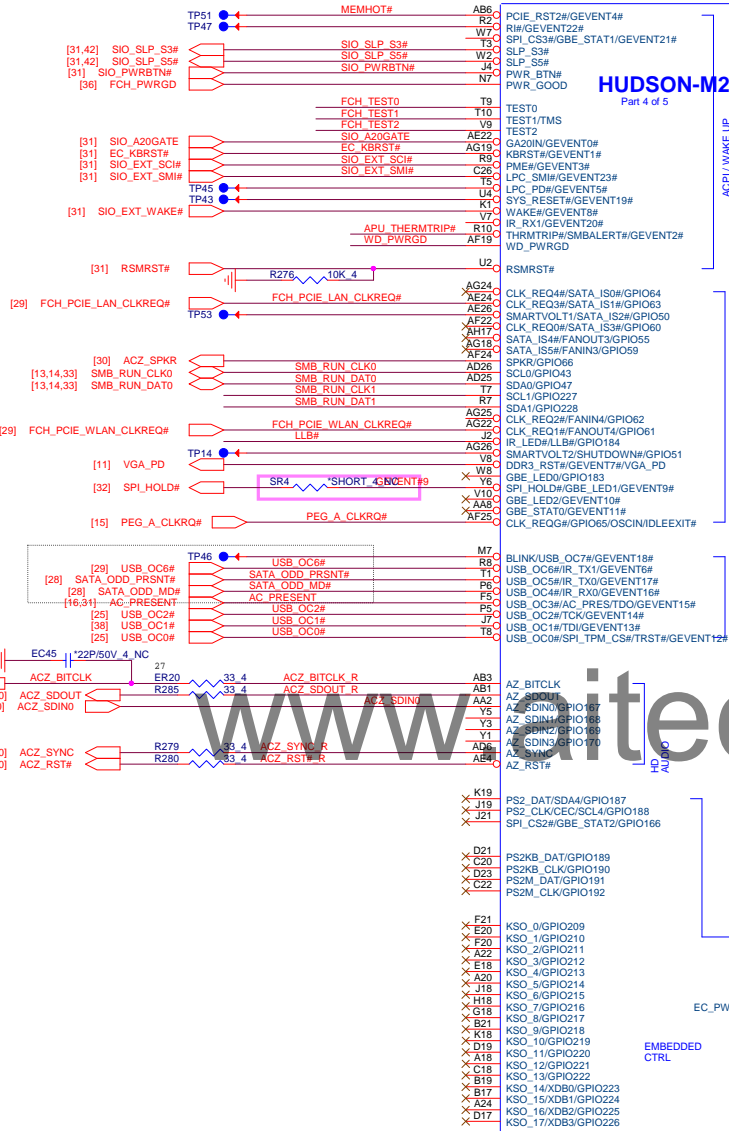
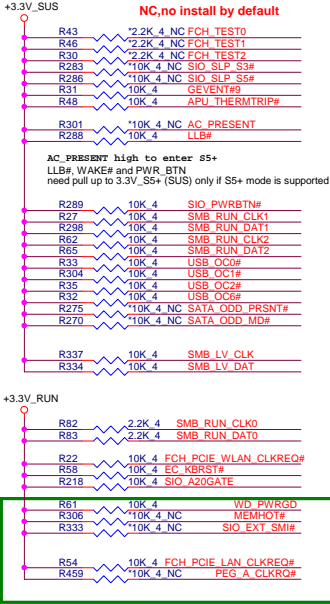
Quanta Computer Inc.
PROJECT : R0AA

Size	Document Number	Rev
	DEBUG&OTHER	B
Date:	Monday, June 25, 2012	Sheet 7 of 55

DEL MEMHOT# Function / +3.3V

USB_OC#

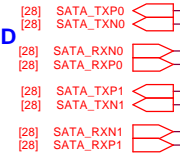
Function	FCH port
USB12 (MB)	USB_OC0#
USB13 (MB)	*USB_OC2#
USB11 (MB)	USB_OC1#
USB10 (I/O)	USB_OC6#



HUNSON M3
M3_100-CK4148(218-0755042)

SATA HDD/SSD

SATA ODD



HUDSON-M2

Part 2 of 5
SD_CLK/SCLK_0/GPIO73
SD_CMD/SLOAD_0/GPIO74
SD_CD#/GPIO75
SD_WP#/GPIO76
SD_DATA0/SDAT1_0/GPIO77
SD_DATA1/SDAT0_0/GPIO78
SD_DATA2/GPIO79
SD_DATA3/GPIO80

GBE_COL
GBE_CRS
GBE_MDCK
GBE_MDIO
GBE_RXCLK
GBE_RXD3
GBE_RXD2
GBE_RXD1
GBE_RXD0
GBE_RXCTL/RXDV
GBE_RXERR
GBE_TXCLK
GBE_TXD3
GBE_TXD2
GBE_TXD1
GBE_TXD0
GBE_TXCTL/TXEN
GBE_PHY_PD
GBE_PHY_RST#
GBE_PHY_INTR

SPI_DI#/GPIO164
SPI_DO#/GPIO163
SPI_CLK#/GPIO162
SPI_CS1#/GPIO165
ROM_RST#/SPI_WP#/GPIO161

VGA_RED
VGA_GREEN
VGA_BLUE

VGA_HSYN#/GPIO68
VGA_VSYN#/GPIO69

VGA_DDC_SDA/GPO70
VGA_DDC_SCL/GPO71

VGA_DAC_RSET
AUX_VGA_CH_P
AUX_VGA_CH_N

AUXCAL

ML_VGA_L0P
ML_VGA_L0N
ML_VGA_L1P
ML_VGA_L1N
ML_VGA_L2P
ML_VGA_L2N
ML_VGA_L3P
ML_VGA_L3N

ML_VGA_HPDI/GPIO229

VIN0/GPIO175
VIN1/GPIO176
VIN2/SDAT1_1/GPIO177
VIN3/SDAT0_1/GPIO178
VIN4/SLOAD_1/GPIO179
VIN5/SCLK_1/GPIO180
VIN6/GBE_STAT3/GPIO181
VIN7/GBE_LED3/GPIO182

NC1
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TEMPIN0/GPIO171
TEMPIN1/GPIO172
TEMPIN2/GPIO173
TEMPIN3/TALERT#/GPIO174

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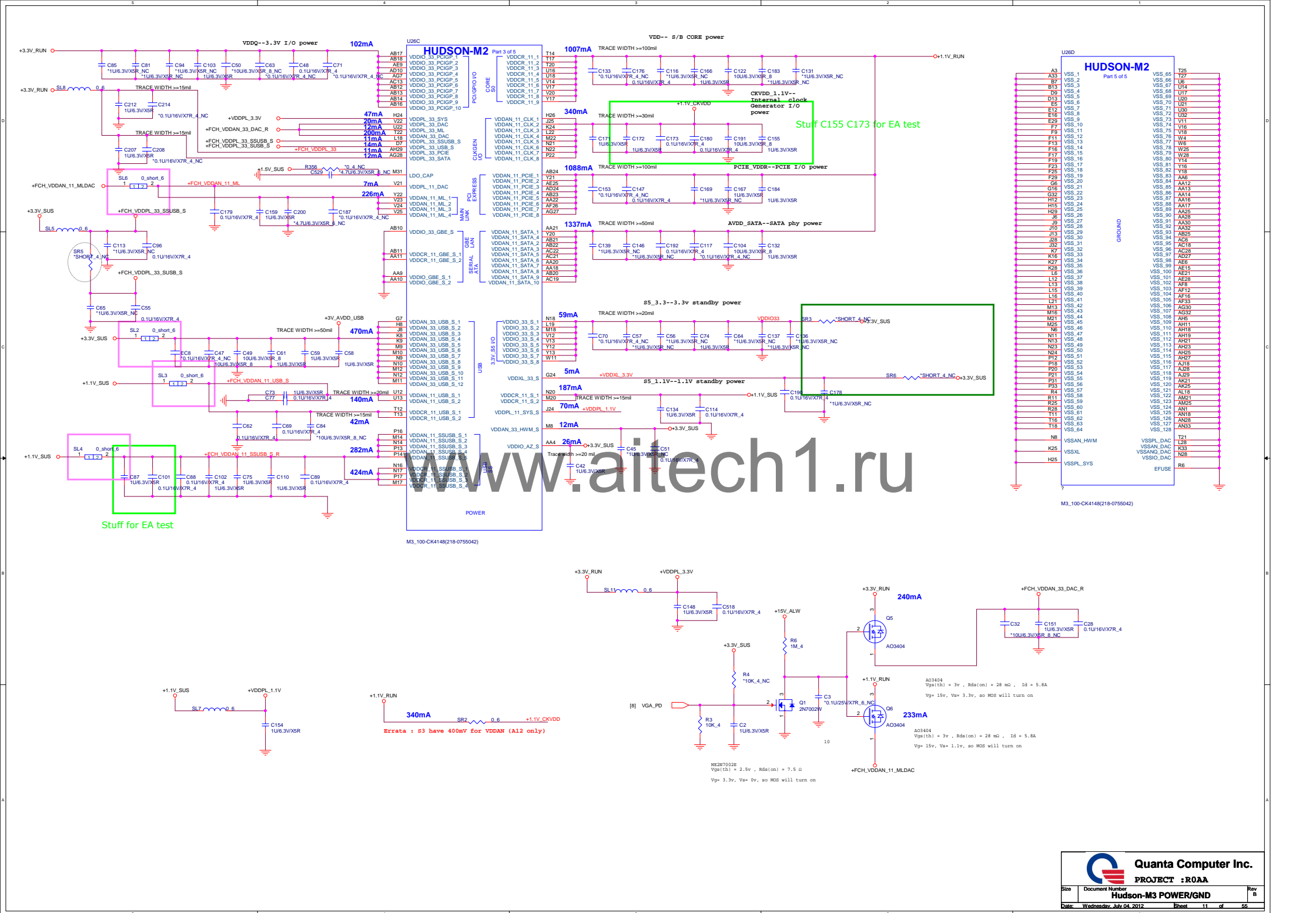
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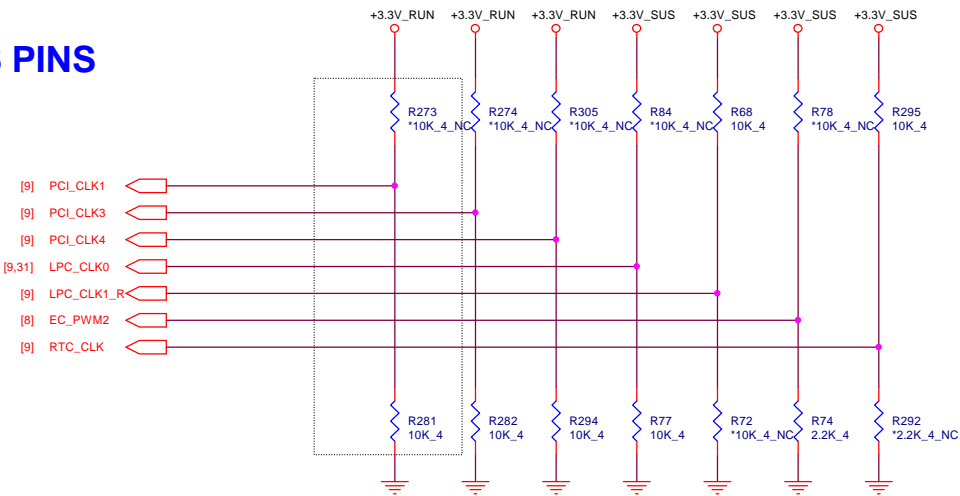
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STRAPS PINS

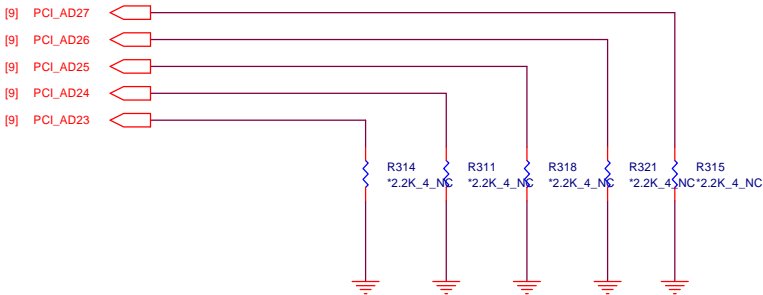


REQUIRED STRAPS

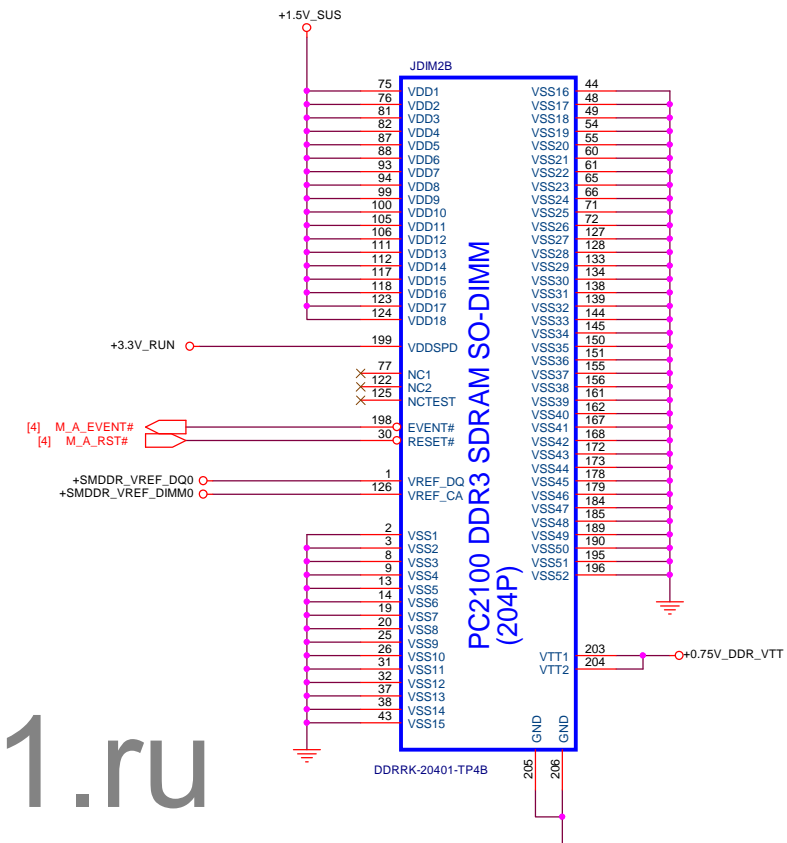
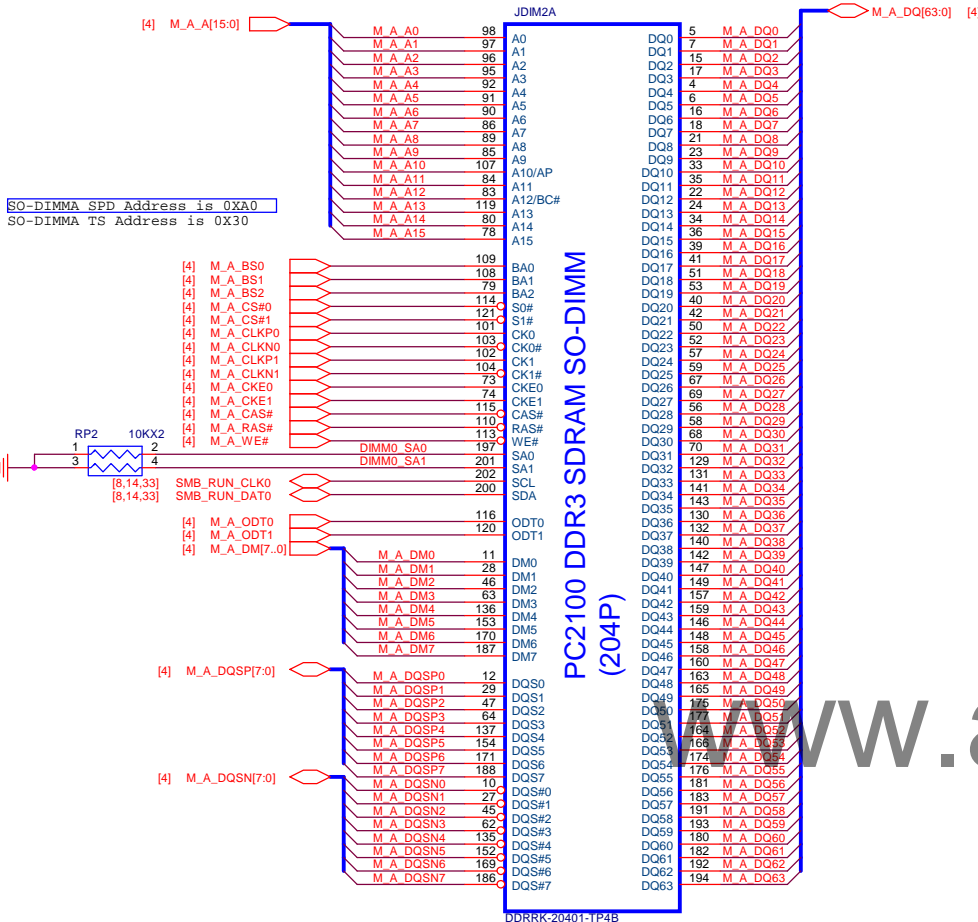
	-----	PCI_CLK1	-----	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	-----	ALLOW PCIe Gen2	-----	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED Setting	LPC ROM	S5 PLUS MODE DISABLED Setting
PULL LOW	-----	FORCE PCIe Gen1 Setting	-----	IGNORE DEBUG STRAP Setting	FUSION CLOCK MODE Setting	EC DISABLED Setting	CLKGEN DISABLED	SPI ROM	S5 PLUS MODE ENABLED Setting

DEBUG STRAPS

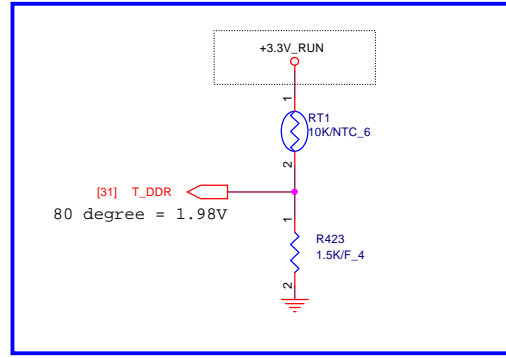
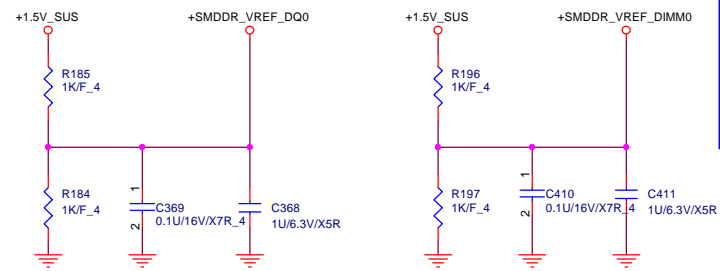
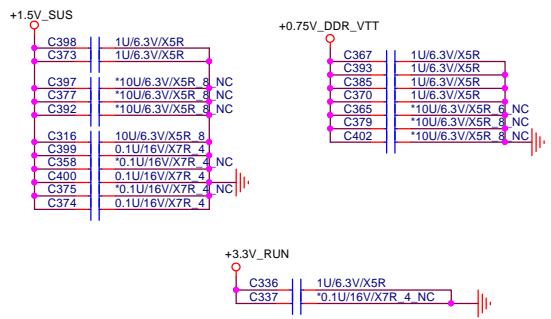
FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]



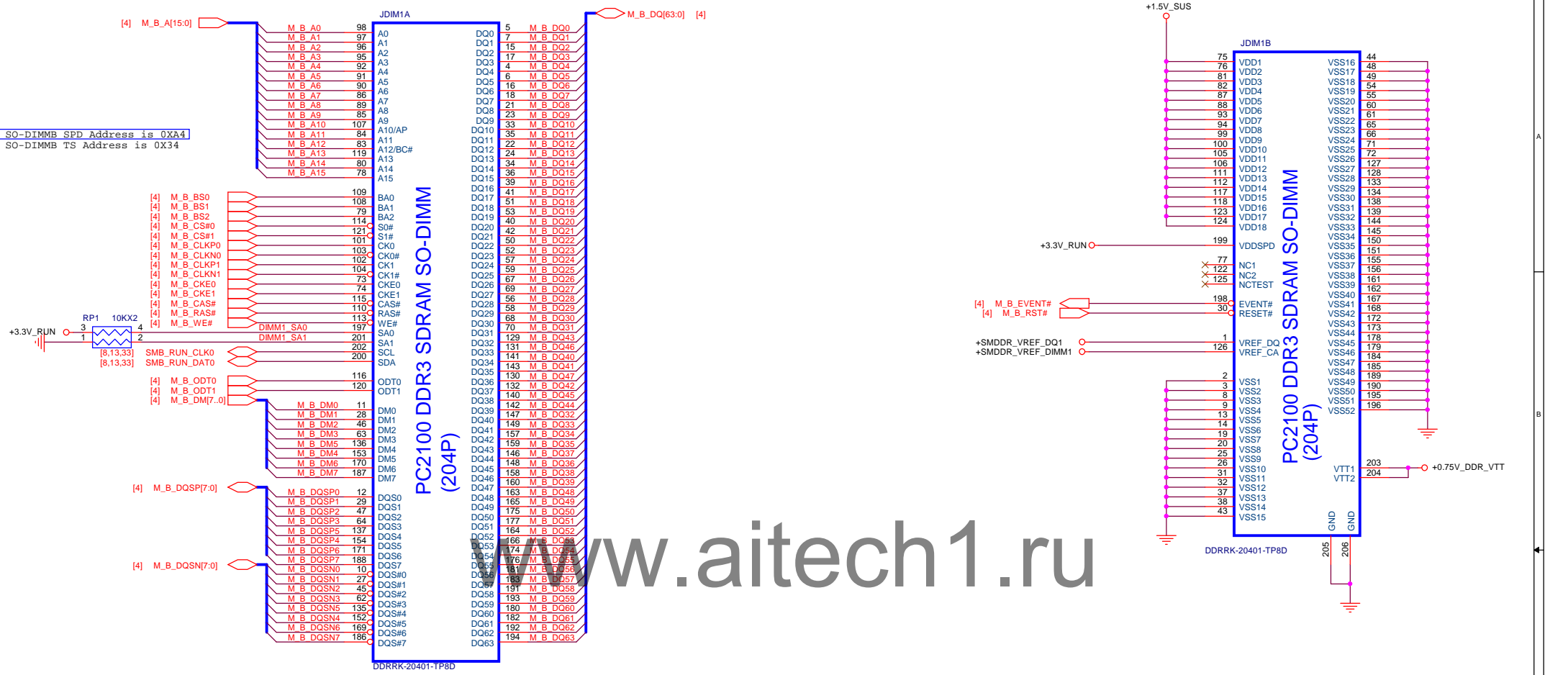
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL Setting	DISABLE ILA AUTORUN Setting	USE FC PLL Setting	USE DEFAULT PCIe STRAPS Setting	DISABLE PCI MEM BOOT Setting
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIe STRAPS	ENABLE PCI MEM BOOT



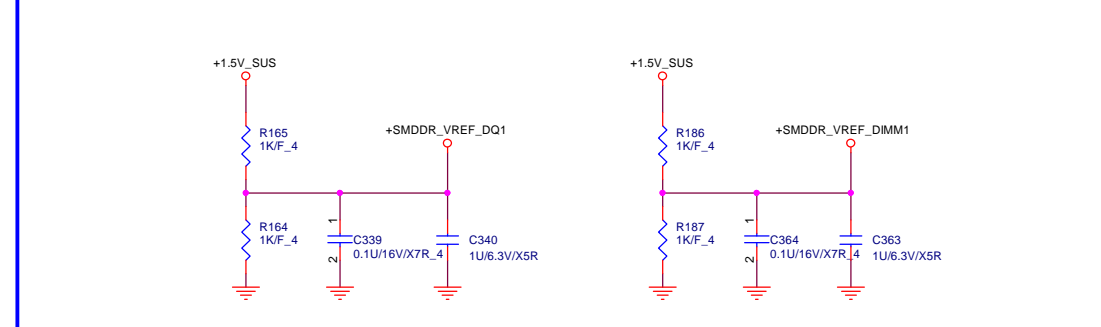
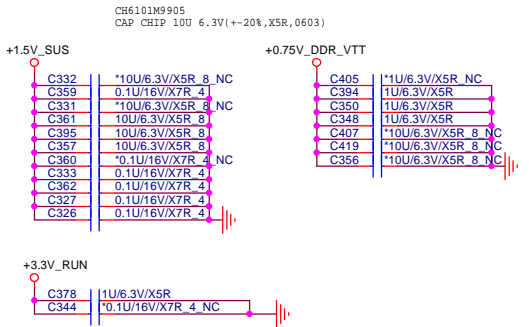
Place these Caps near So-Dimm0.

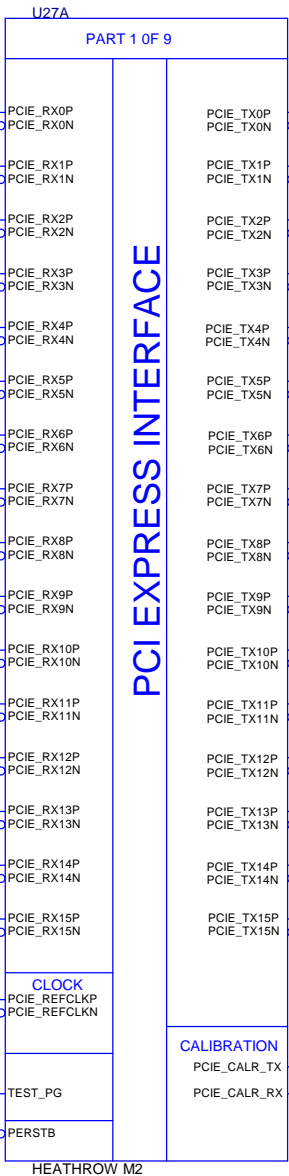


SO-DIMMB SPD Address is 0XA4
SO-DIMMB TS Address is 0X34



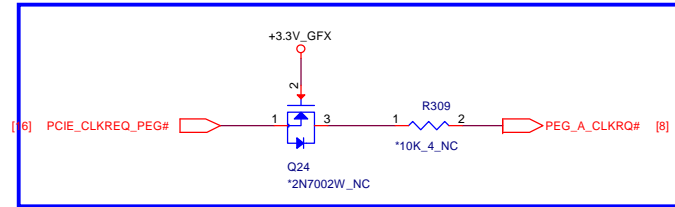
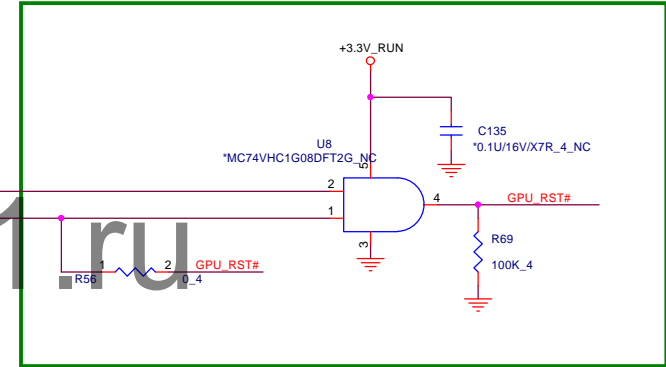
Place these Caps near So-Dimm1.





Thames/Whistler/Seymour PCIe-Gen2
0.1uF AC coupling Caps for PCIe GEN1/2

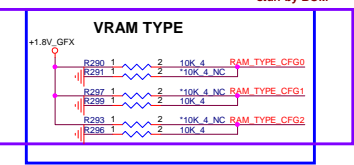
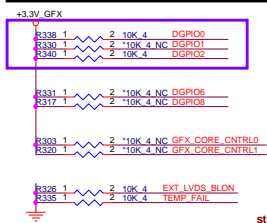
Part Description,
Part Number,
Footprint need update



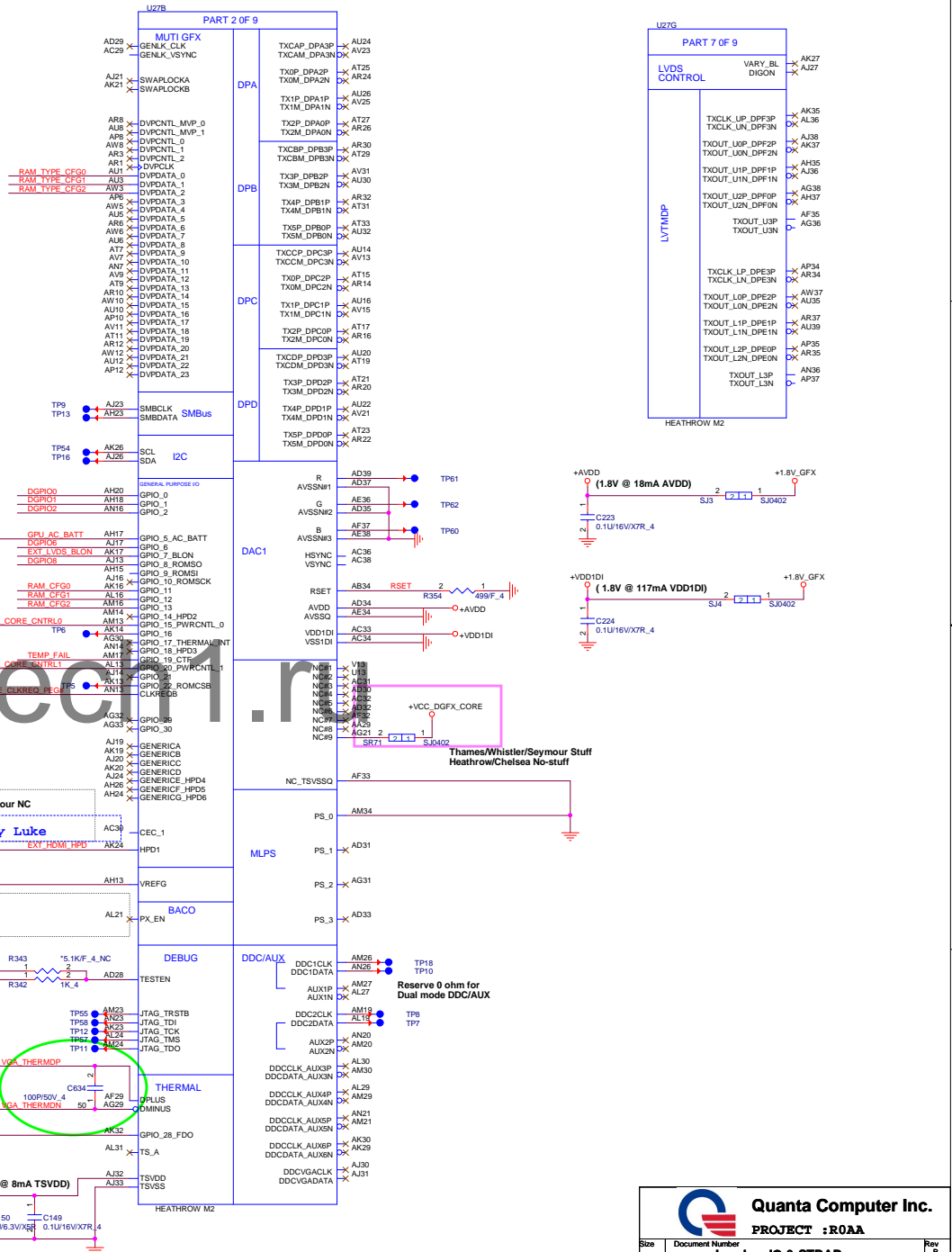
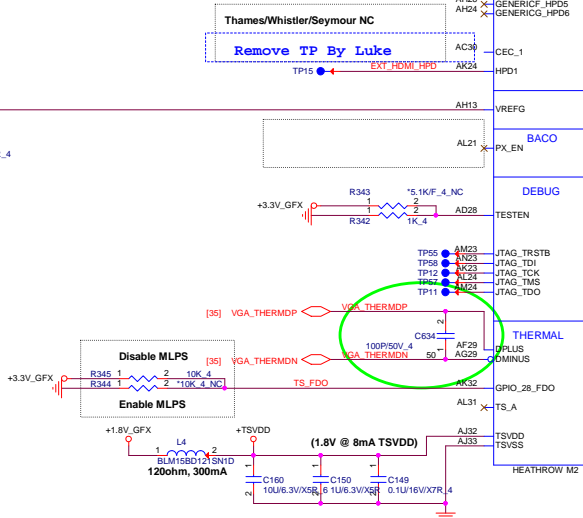
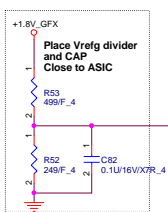
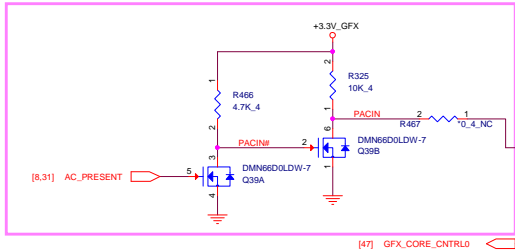
Support Themas & Seymour only

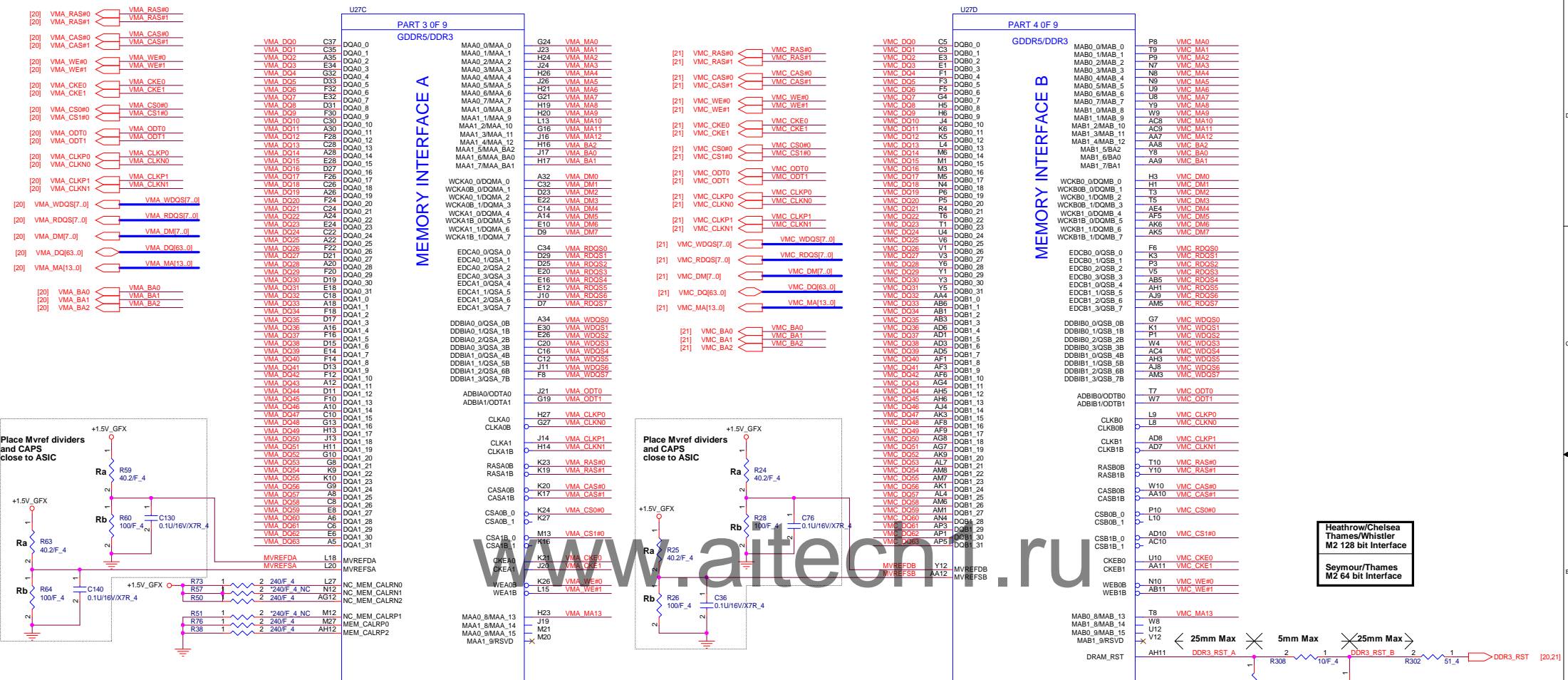
CONFIGURATION STRAPS			
STRAPS	PIN	DESCRIPTION	SET
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING 0 = 50% Tx output swing 1 = Full Tx output swing	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = Disable ; 1 = Enable	0
BIF_GEN3_EN_A	GPIO2	PCIE Gen2 Enable 0 = GEN2 not supported at power-on 1 = GEN2 supported at power-on	1
BIF_VGA_DIS	GPIO9	0: VGA Controller capacity enabled 1: VGA Controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 = Disable ; 1 = Enable	0
AUD[1] AUD[0]	VGAHSYNC VGAHSYNC	AUD[1:0]: 00 - No audio function; 01 - Audio for DisplayPort only; 10 - Audio for DisplayPort and HDMI if dongle is detected; 11 - Audio for both DisplayPort and HDMI.	00
CEC_DIS	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0 = Disable ; 1 = Enable	0
RESERVED RESERVED RESERVED RESERVED	GENLK_CLK GPIO8 GPIO21 GENERIC	Allow for Pull-up PADS for the reserved straps but do not install resistor if these GPIOs are used, they must keep low and not conflict during reset RESERVED RESERVED RESERVED Reserved (for Thames/Whistler/Seymour only)	

APERTURE SIZE				
MEMORY APERTURE SIZE SELECT				
MEMORY SIZE	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11	
128MB	0	0	0	
256MB	0	0	1	
64MB	0	1	0	



Memory Straps	RAM_TYPE_CFG2	RAM_TYPE_CFG1	RAM_TYPE_CFG0	Quanta PN (QuantaBuy)	Vendor PN	Support GPU
900MHz Samsung 1GB(64M*16*8pcs)	0	0	1	AKD5EGGT509	K4W1G1646G-Bc11	For Thames
900MHz Hynix 1GB(64M*16*8pcs)	0	1	0	AKD5LZW7W07	H5TQ1G63DFR-11C	For Thames
900MHz Micron 1GB(64M*16*8pcs)	1	0	0	AKD5EGSTL01	MT41J64M16JT	For Thames






	L27	N12	AG12	M12	M27	AH12
Heathrow/Chelsea	NC	NC	NC	NC	Stuff 120	Stuff 120
Thames/Whistler	Stuff 240	NC	Stuff 240	NC	Stuff 240	Stuff 240
Seymour	NC	Stuff 240	NC	Stuff 240	NC	NC

GPU (Pkg)	Preliminary Branding*	Memory Size	Mem Width	Memory Type	Mem Devices	Pro Perf (TDP)*	XT Perf (TDP)*
Chelsea (M2)	HD 7700	2 GB	128bit	128M x16 DDR3	8 pcs	P5500 (25W)	P5800 (35W)
	HD 7700	1 GB	128bit	64M x16 DDR3	8 pcs	P5500 (25W)	P5800 (35W)
Thames (M2)	HD 7600	2GB	128bit	128M x16 DDR3	8 pcs	P4600 (18W)	P5200 (22W)
	HD 7600	1GB	128-bit	64M x16 DDR3	8 pcs	P4600 (18W)	P5200 (22W)
	HD 7500	1GB	64-bit	128M x16 DDR3	4 pcs	P3000 (15W)	P3200 (18W)

GPU (Pkg)	Series Branding*	Mem Size	Mem width	Mem Type	Mem Devices	Pro Perf (TDP)*	XT Perf (TDP)*
Thames (M2)	HD 7600	1 GB	64-bit	128Mx16 GDDR5	(4pcs)	P3800 (18W)	-
	HD 7700	2 GB	128-bit	128Mx16 GDDR5	(8 pcs)	P6600 (25W)	P7500 (35W)
Chelsea (M2)	HD 7700	1 GB	128-bit	64Mx16 GDDR5	(8 pcs)	P6600 (25W)	P7500 (35W)
	HD 7800	2 GB	128-bit	128Mx16 GDDR5	(8 pcs)	P8000 (35W)	P9500 (45W)
Heathrow (M2)	HD 7800	1 GB	128-bit	64Mx16 GDDR5	(8 pcs)	P8000 (35W)	P9500 (45W)

GPU	Series Branding*	Mem Size	Mem width	Mem Type	Mem Devices	Pro Perf (TDP)*	XT Perf (TDP)*
Seymour GTX (M2)	HD 7400	512 MB	64-bit	64Mx32 GDDR5	(2pcs)	P2700 (20W)	-
	HD 7600	1 GB	128-bit	64Mx32 GDDR5	(4pcs)	P5200 (22W)	-
Thames (M2)	HD 7600	512 MB	64-bit	64Mx32 GDDR5	(2pcs)	P3800 (18W)	P4200 (25W)
	HD 7700	1GB	128-bit	64Mx32 GDDR5	(4pcs)	P6600 (25W)	P7500 (35W)
Chelsea (M2)	HD 7700	512 MB	128-bit	32Mx32 GDDR5	(4pcs)	P6600 (25W)	P7500 (35W)
	HD 7800	1GB	128-bit	64Mx32 GDDR5	(4pcs)	P8000 (35W)	P9500 (45W)



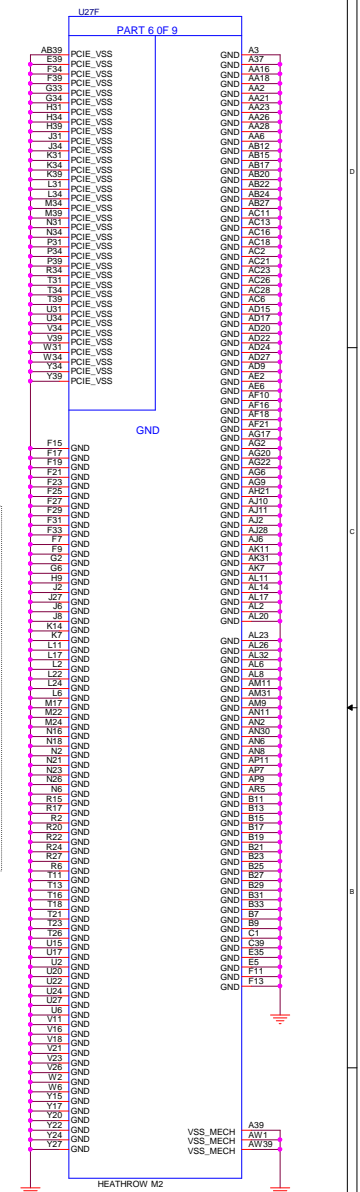
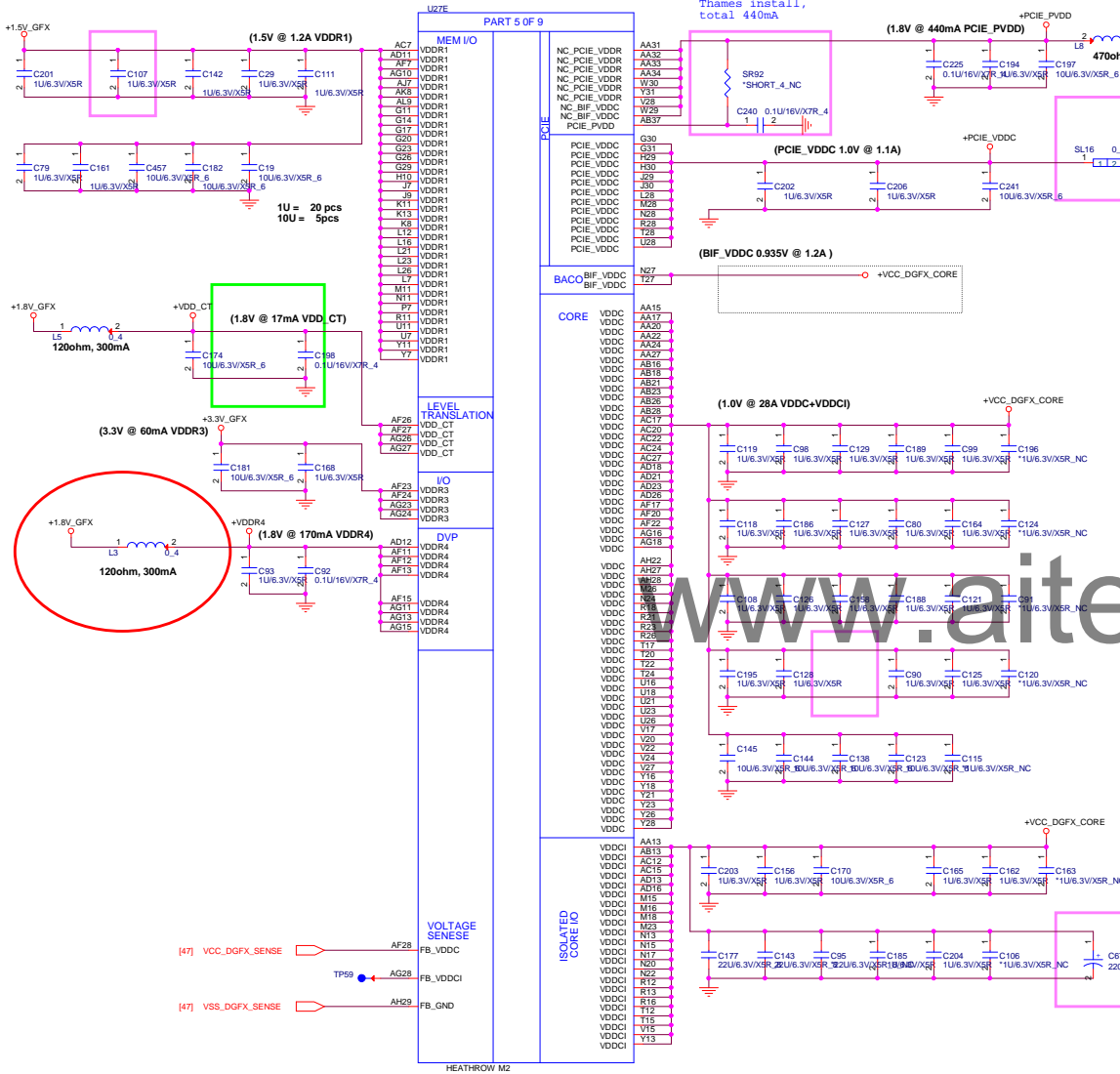
Quanta Computer Inc.
PROJECT : R0AA

Size	Document Number	London_MEMORY	Rev	B
Date:	Monday, June 25, 2012	Sheet	17	of 55

For Thames/Whistler/Seymour
NC_Pcie_VDDR and NC_BIF_VDDC
should be tied with PCIE_PVDD
consumption about 440mA

Chelsea uninstall
Thames install,
total 440mA

Del BACO circuit

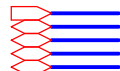



```
[17] VMA_MA[13..0]
[17] VMA_DQ[63..0]
[17] VMA_DM[7..0]
[17] VMA_WDQS[7..0]
[17] VMA_RDQS[7..0]
```

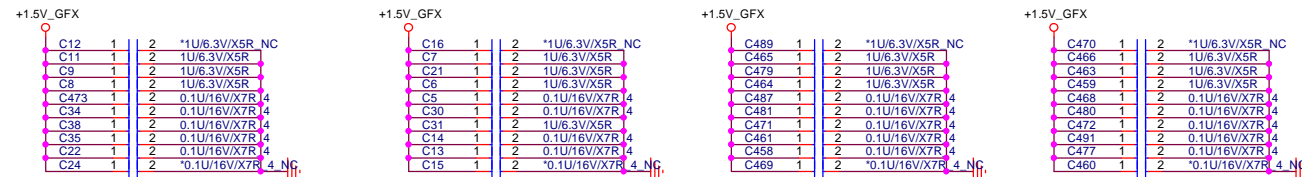


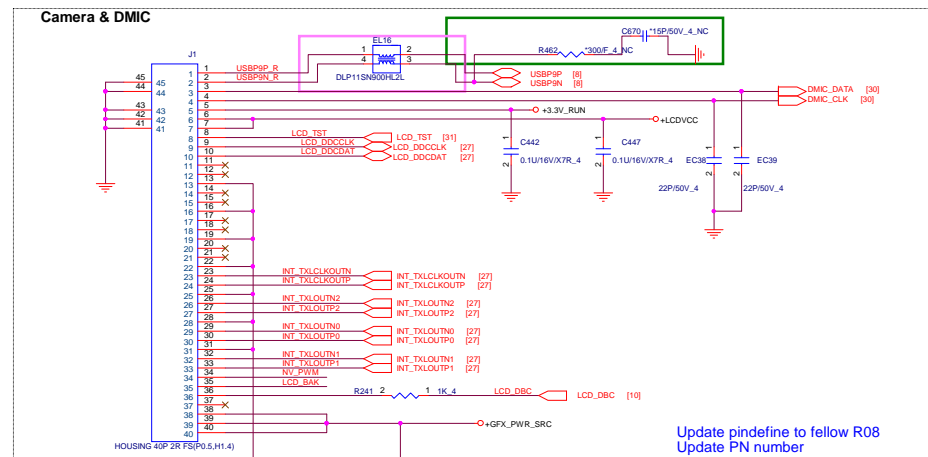
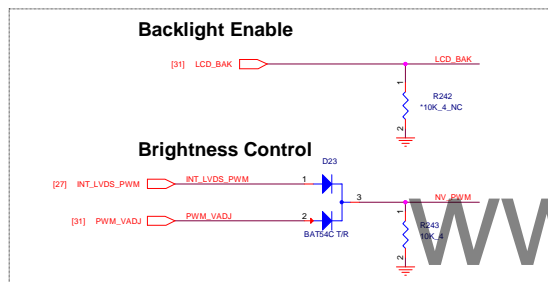
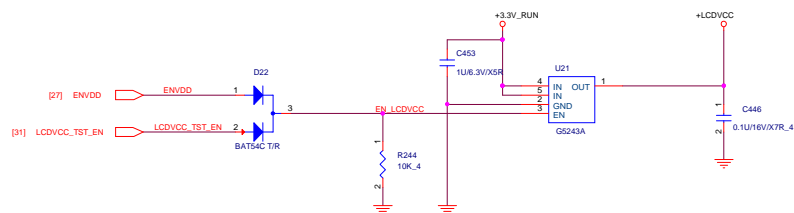
Quanta Computer Inc.
PROJECT : R0AA


```
[17] VMC_MA[13..0]
[17] VMC_DQ[63..0]
[17] VMC_DM[7..0]
[17] VMC_WDQS[7..0]
[17] VMC_RDQS[7..0]
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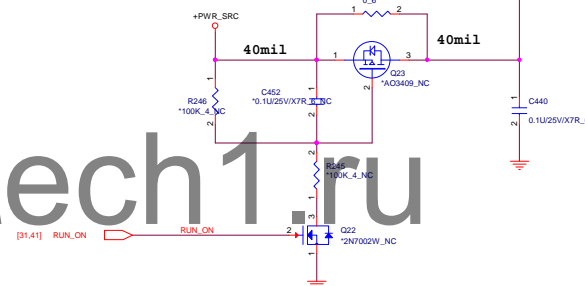
VMC_CLKP0 R8 2 1 56.4
VMC_CLKN0 R9 2 1 56.4
VMC_CLKP1 R257 2 1 56.4
VMC_CLKN1 R256 2 1 56.4



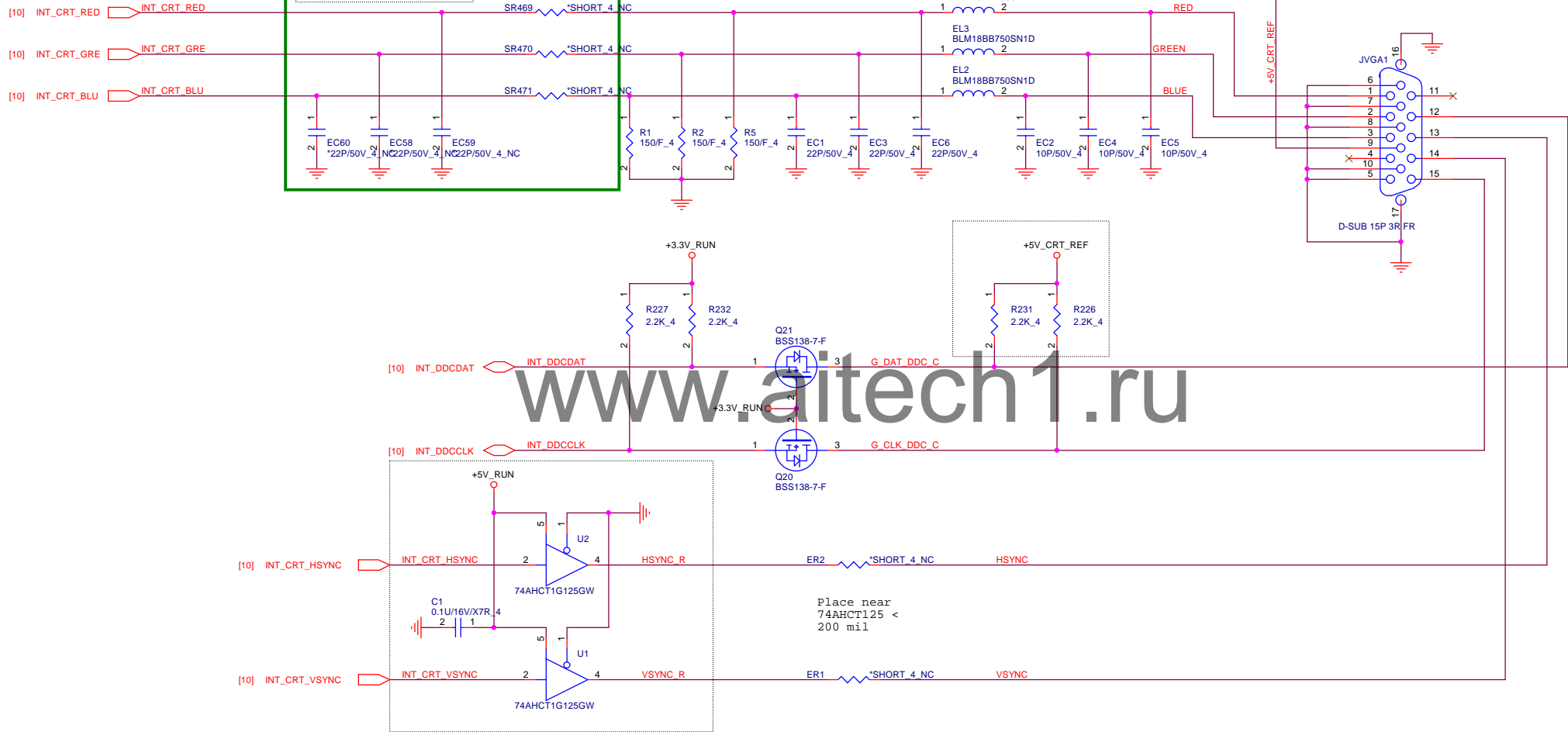


EMC Reserve

INT_TXCLKOUTN	ER18_1	2	3.3P	INT_TXCLKOUTP
INT_TXLOUTN2	ER18_1	2	3.3P	INT_TXLOUTP2
INT_TXLOUTN0	ER17_1	2	3.3P	INT_TXLOUTP0
INT_TXLOUTN1	ER19_1	2	3.3P	INT_TXLOUTP1



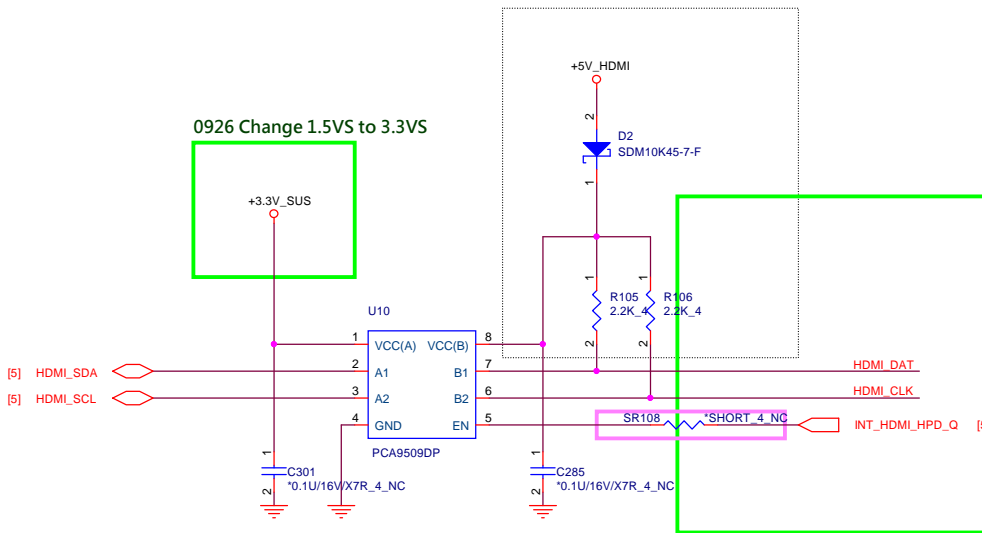
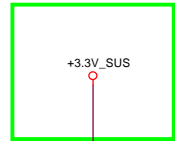
Layout Note:
Setting R,G,B treac
impedance to 50 ohm.



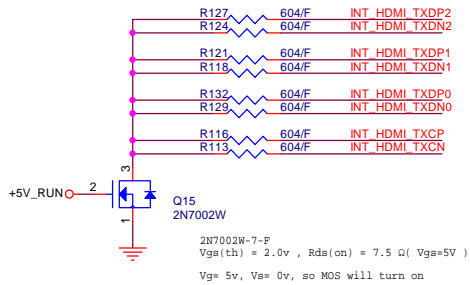
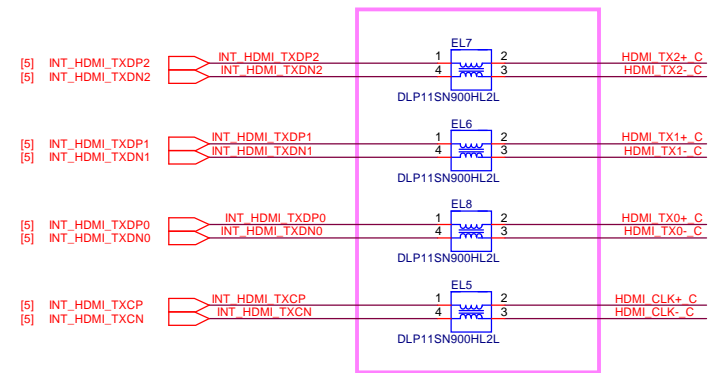
Quanta Computer Inc.
PROJECT : R0AA

Size	Document Number	Rev
	VGA Conn	B
Date:	Friday, June 29, 2012	Sheet 23 of 55

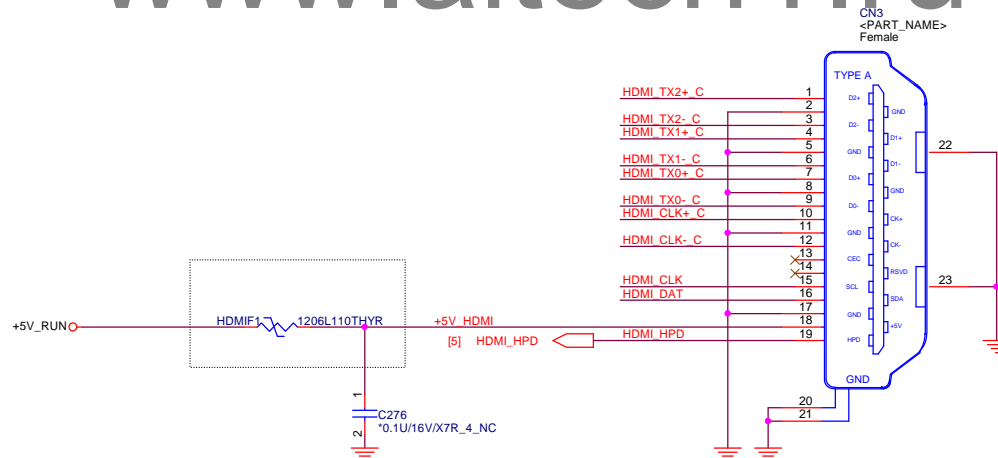
0926 Change 1.5VS to 3.3VS



Reserve for EMI and close to HDMI CONN



www.aitech1.ru HDMI Conn.



Quanta Computer Inc.

PROJECT : R0AA

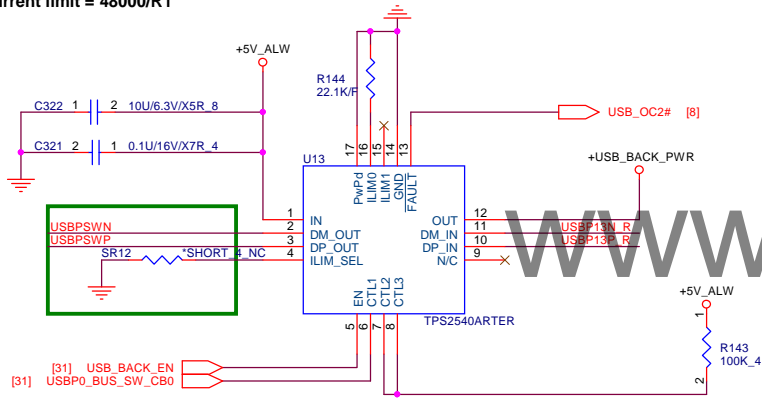
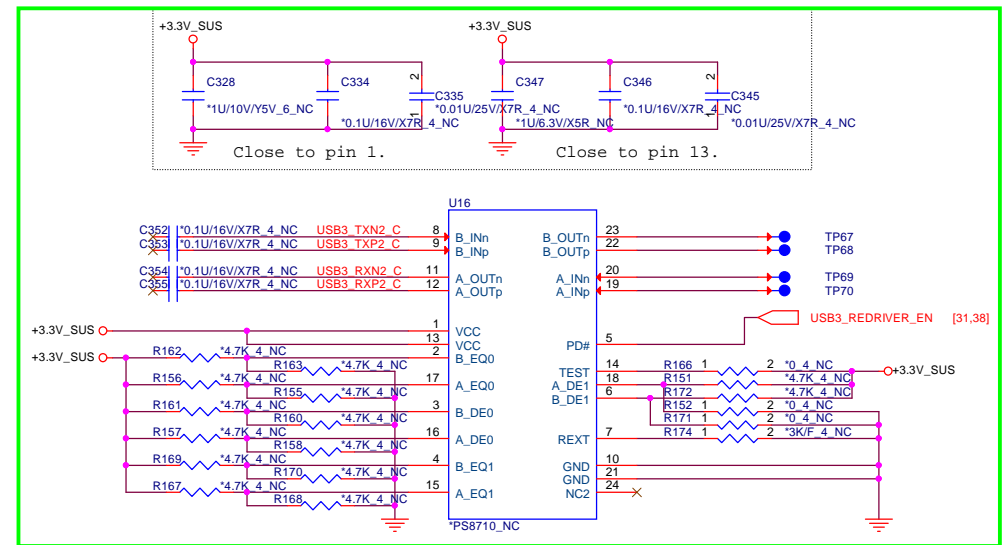
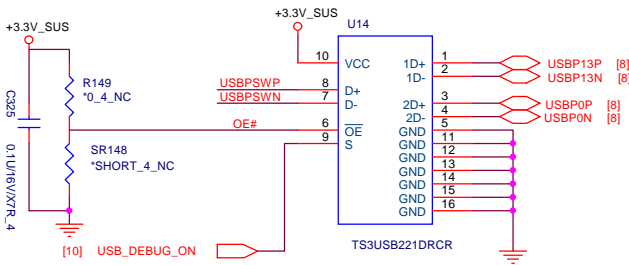
S	OE	Function
X	H	Disconnect
L	L	D=1D
H	L	D=2D

USB Power share

USBP0_BUS_SW_CB0	Mode
Low	DCP, Auto-detect
High	CDP, BC Spec 1.1

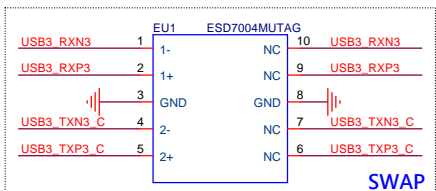
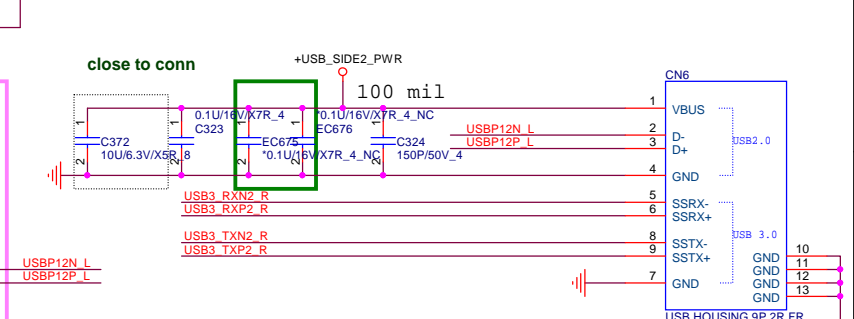
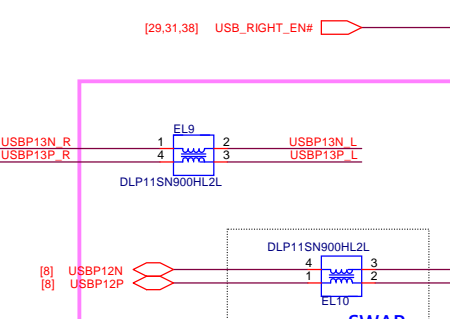
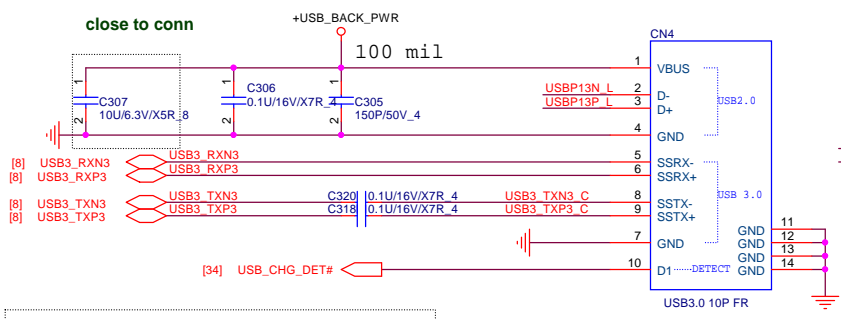
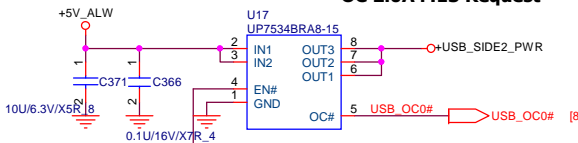
	R1	mA
OC limitation	100k ohm	480
	22.1k ohm	2171

Current limit = 48000/R1

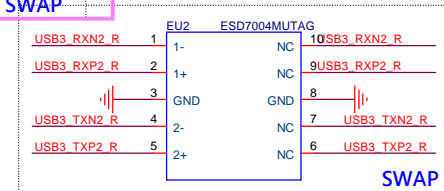
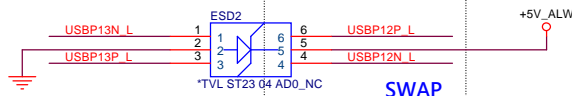


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I continuous 1.5A
OC 2.0A M13 Request

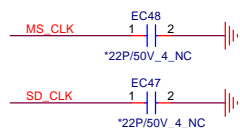
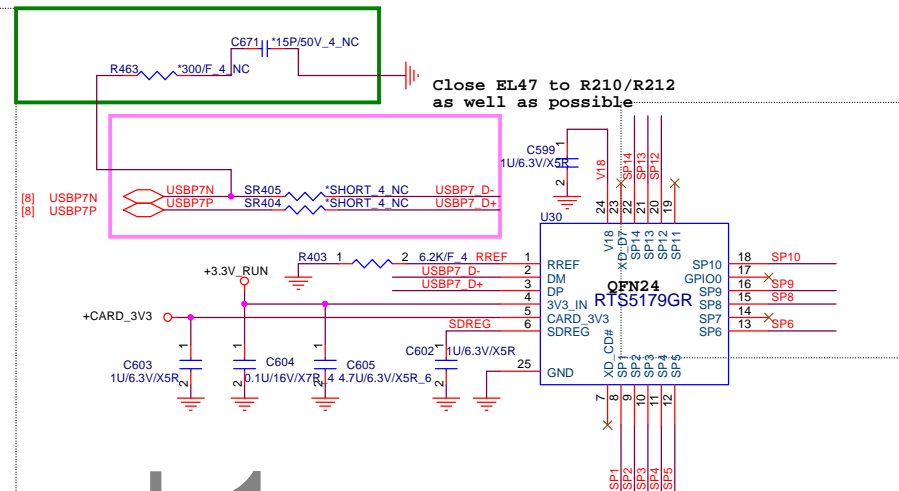
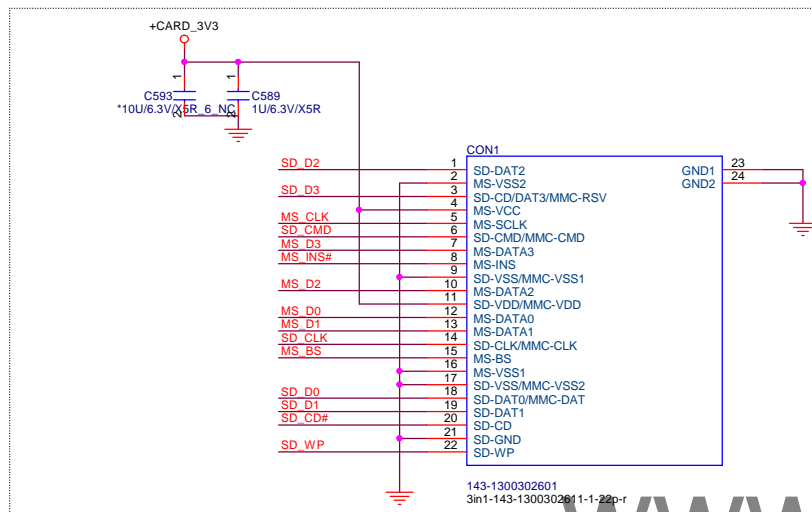


ESD Function
Place ESD diodes as close as USB connector.



Cardreader (RTS5179GR) Support SD3.0 USH50

Change CON1 footprint to 3in1-143-1300302611-1-22p-r(follow R09)



SP1	SD_WP	MS_CLK
SP2		MS_INS#
SP3	SD_D1	
SP4	SD_D0	MS_D7
SP5	SD_D7	MS_D3
SP6	SD_CD#	
SP8	SD_CLK	MS_D2
SP9	SD_D5	MS_D0
SP10	SD_CMD	
SP12	SD_D3	MS_D1
SP13	SD_D2	MS_D5
SP14		MS_BS

Share Pin

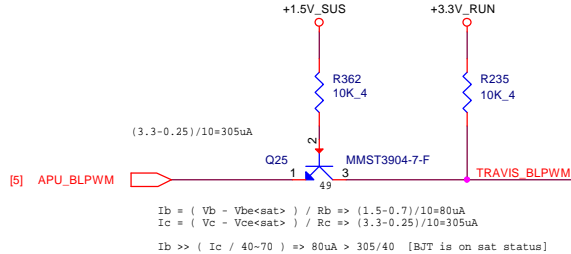
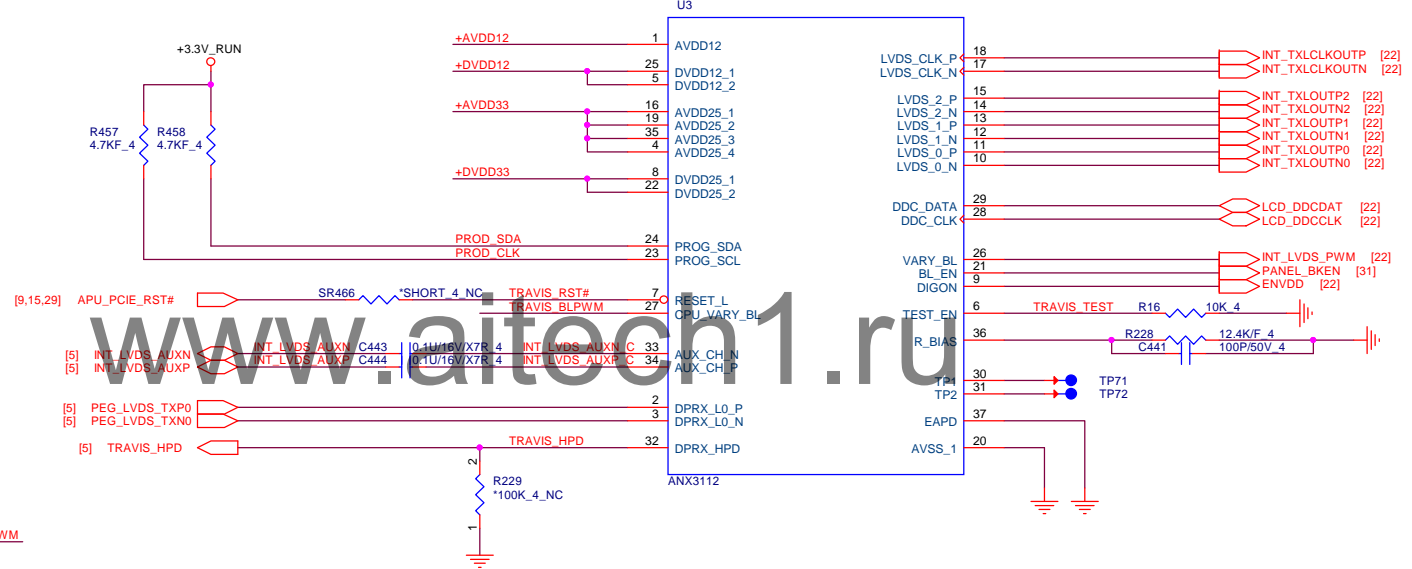
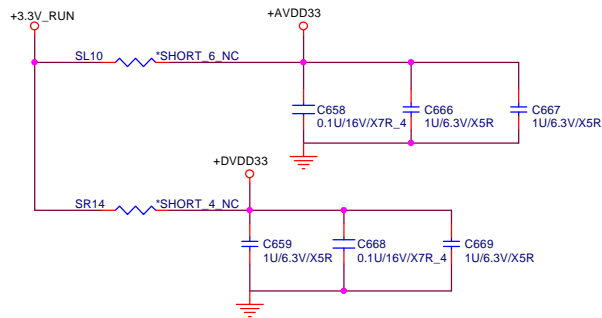
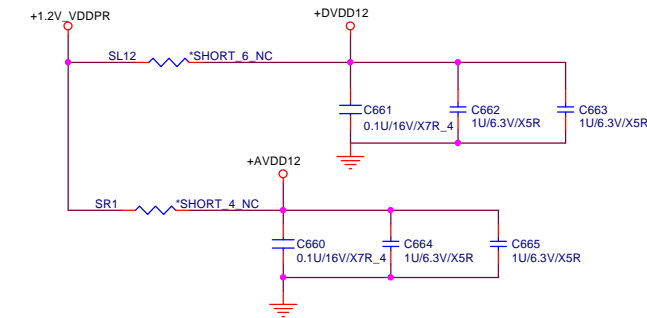
	SD_CARD	MS_CARD
SP1	SW_WP	MS_CLK
SP2		MS_INS#
SP3	SD_D1	
SP4	SD_D0	MS_D7
SP5	SD_D7	MS_D3
SP6	SD_CD#	
SP7	SD_D6	MS_D6
SP8	SD_CLK	MS_D2
SP9	SD_D5	MS_D0
SP10	SD_CMD	
SP11	SD_D4	MS_D4
SP12	SD_D3	MS_D1
SP13	SD_D2	MS_D5
SP14		MS_BS



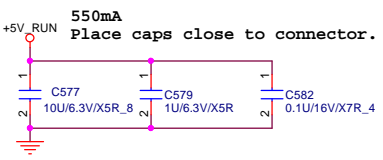
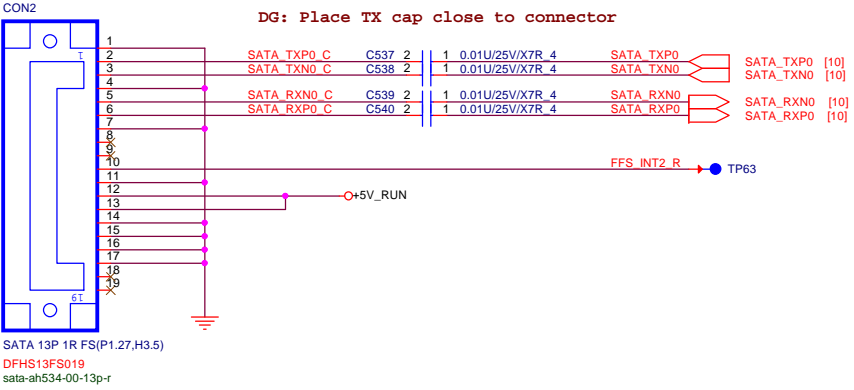
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PROJECT : R0AA

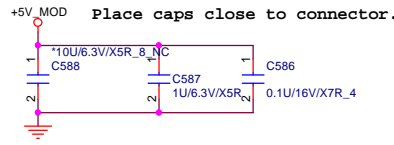
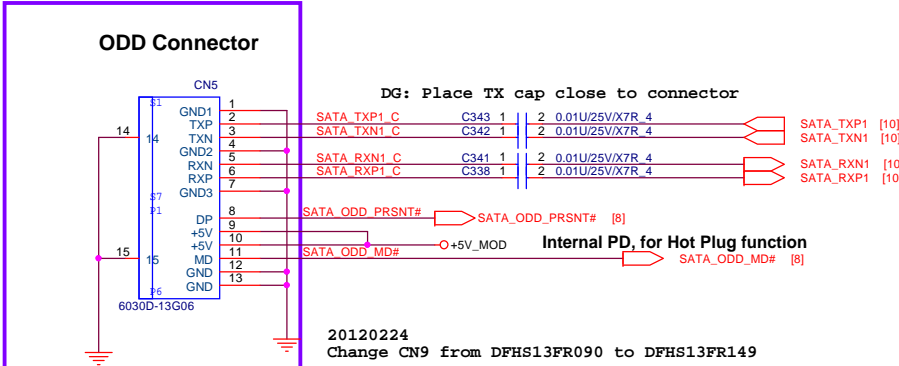
Size	Document Number	Rev
	Cardreader (RTS5179GR)	1A
Date:	Thursday, June 28, 2012	Sheet 26 of 55



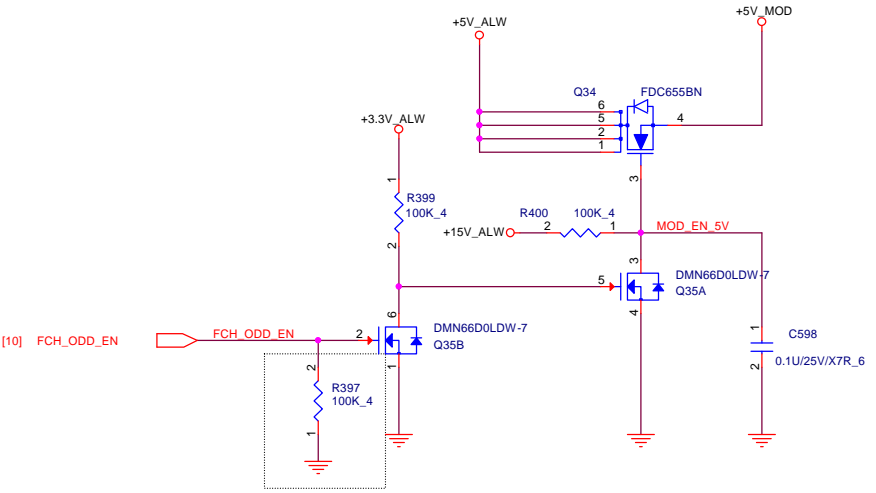
HDD

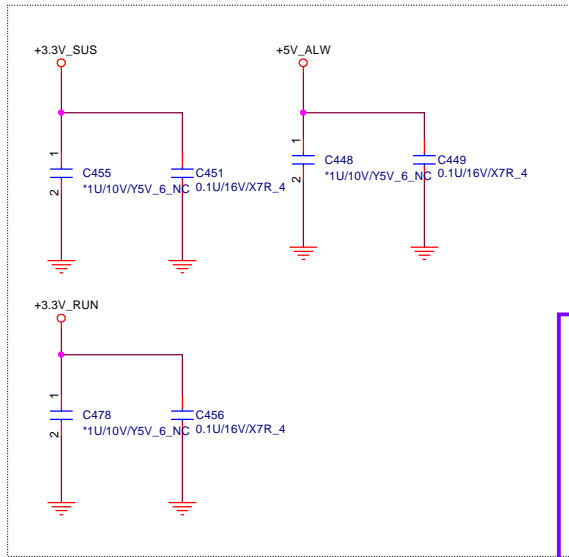


ODD

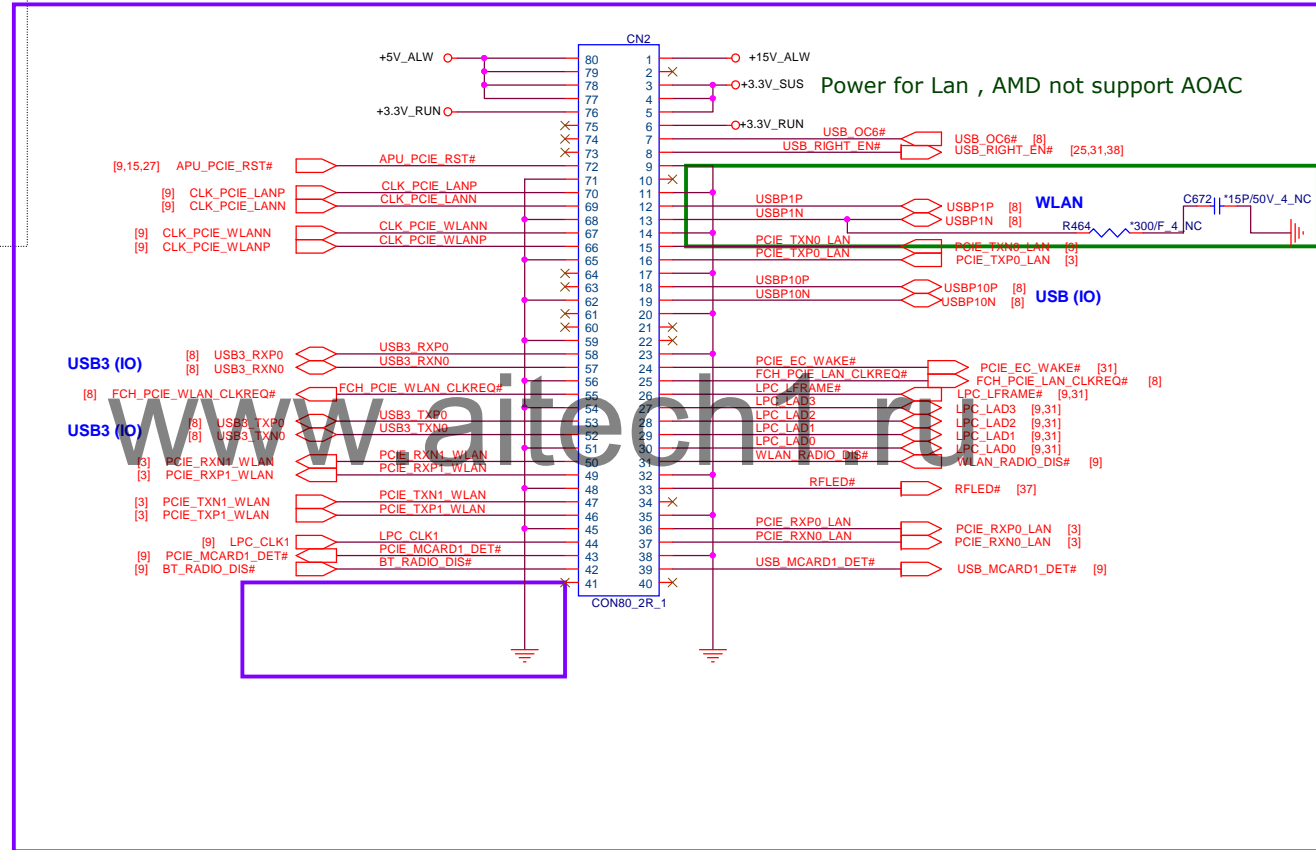


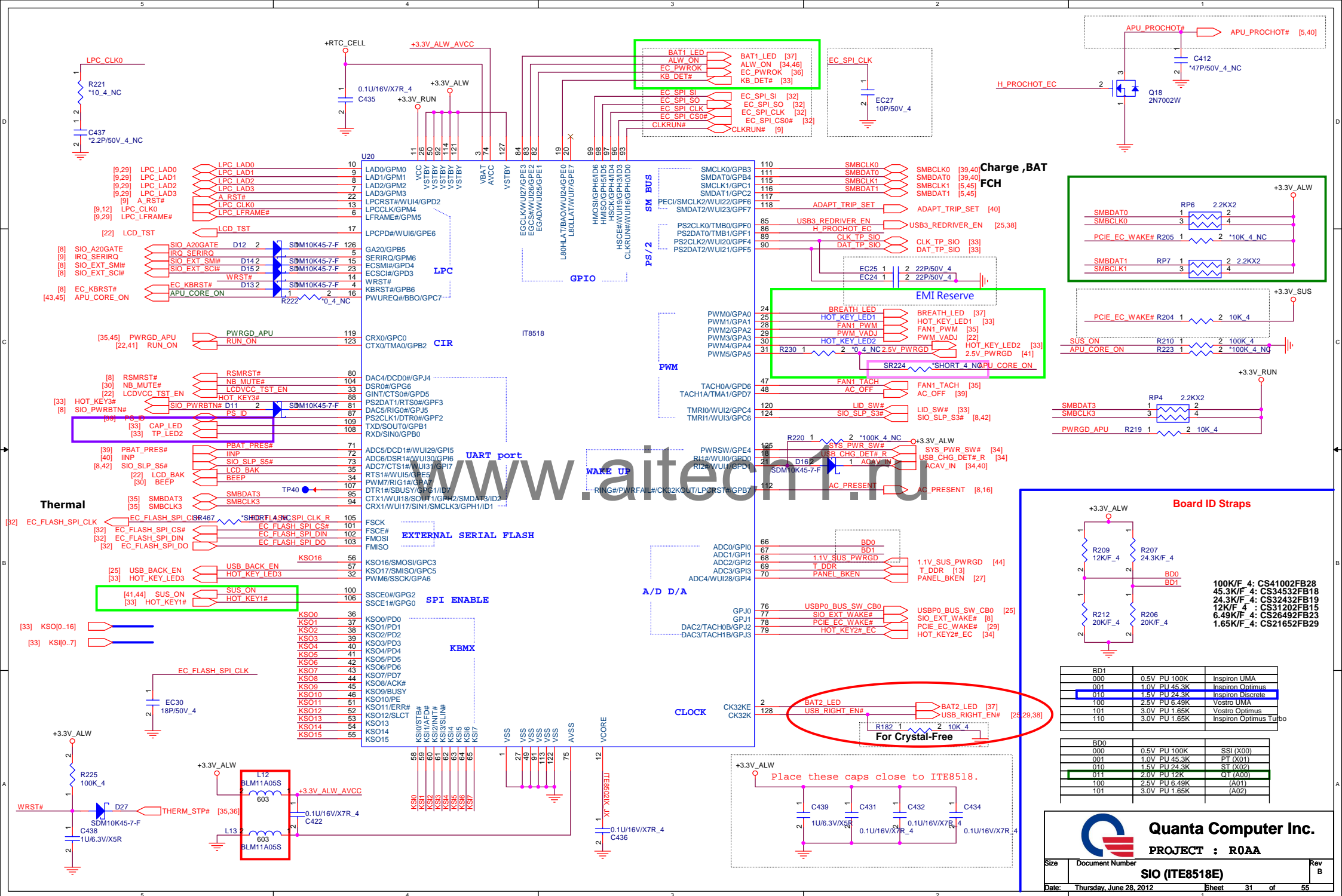
Support Zero power ODD





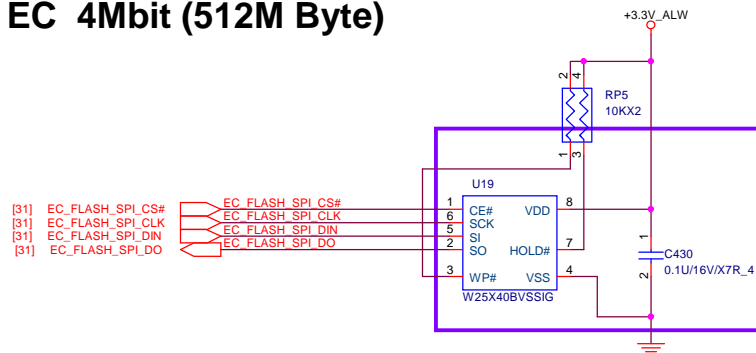
20120229
Change CN9 footprint from "88161-08001-80p-ldh" to "88069-8001b-bs-80p-ldh-smt"



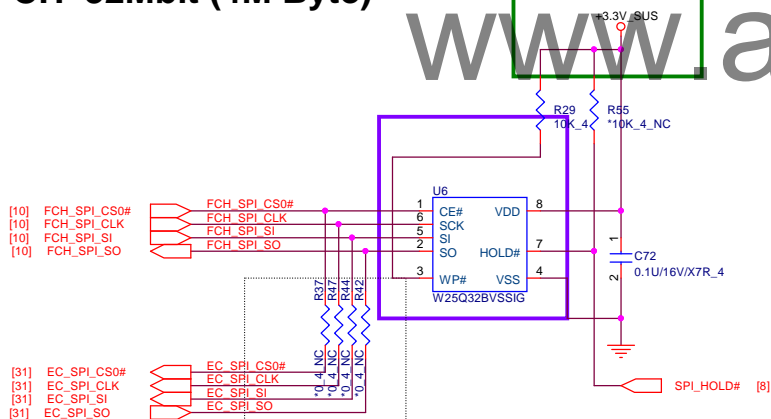


FLASH / RTC

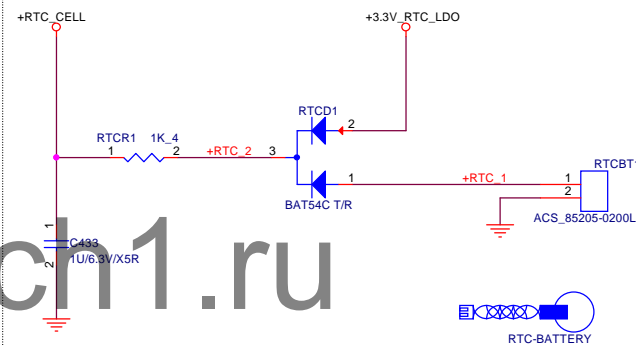
For EC 4Mbit (512M Byte)



For FCH 32Mbit (4M Byte)

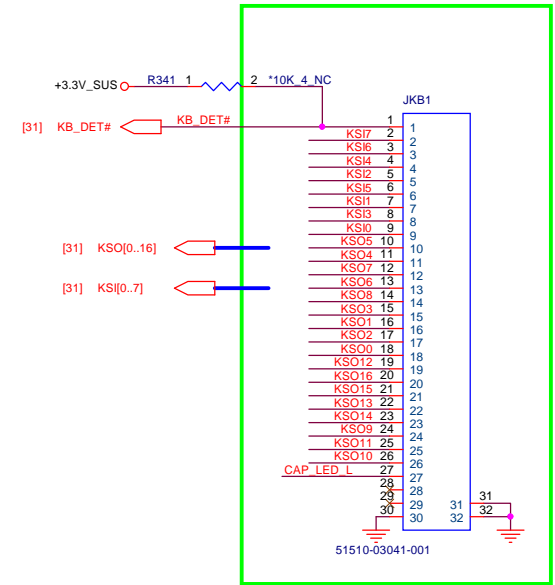


RTC

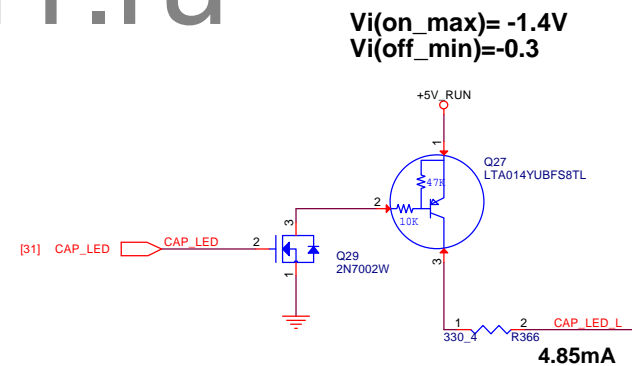


Double, 25'C, Vf=0.4V, If=25mA
one, 25'C, Vf=0.35V, If=15.8mA

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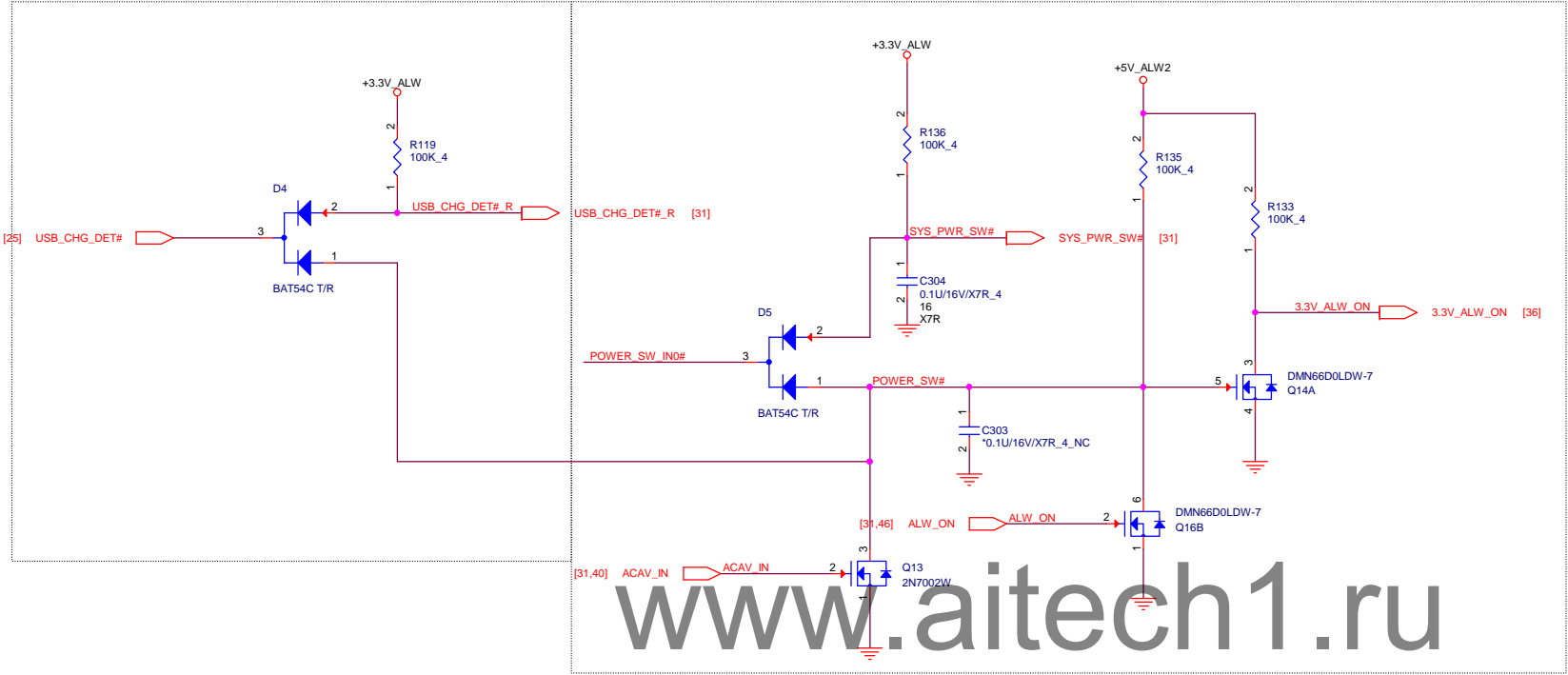


Change JKB1 PN to DFFC30FR075



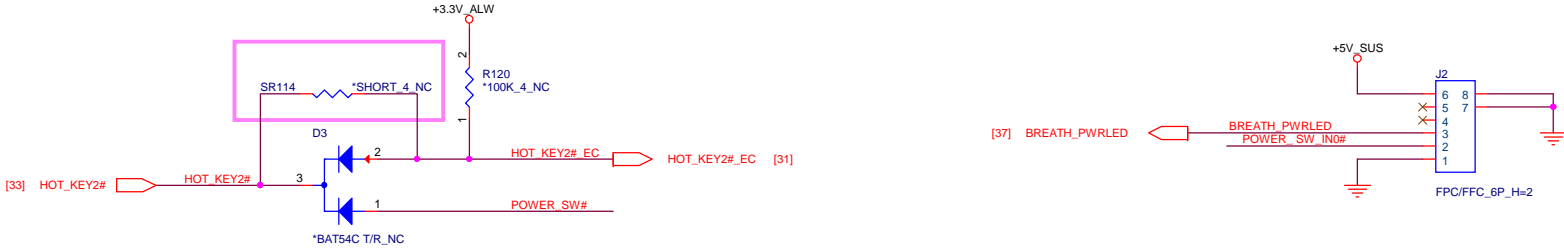
For USB charger usage

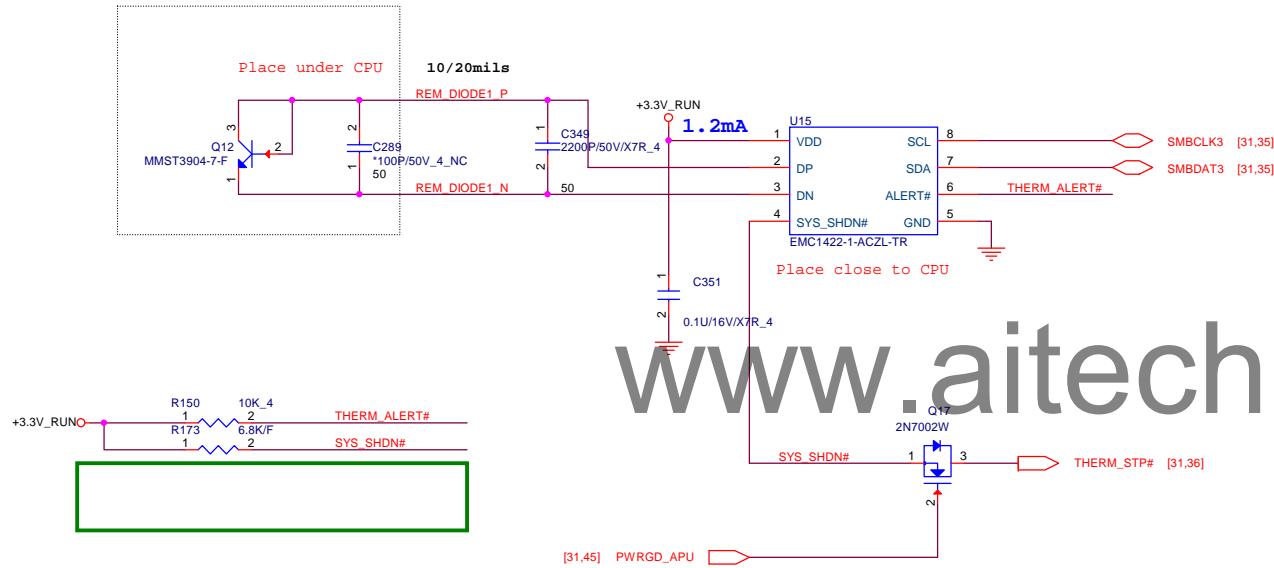
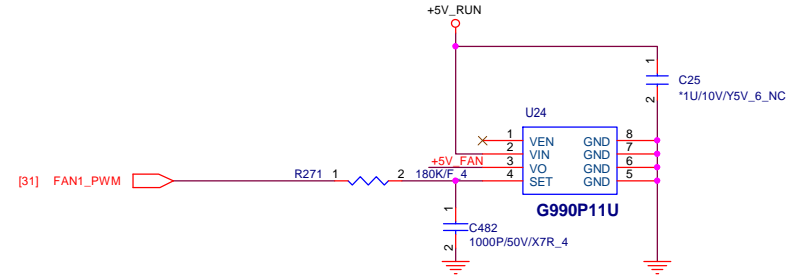
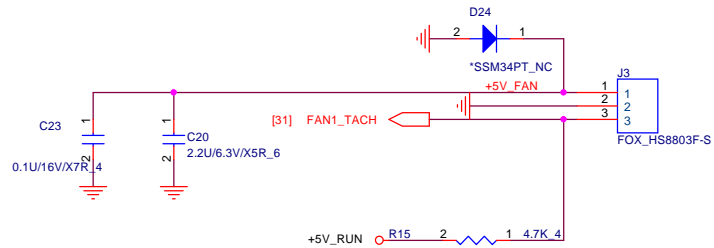
3V ALW ON POWER LOGIC



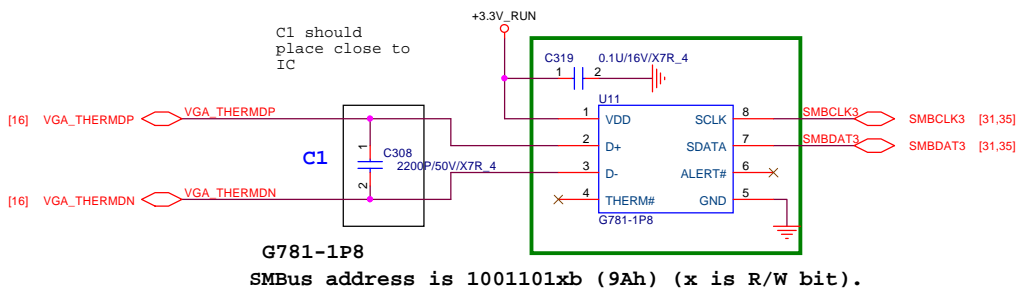
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TO PWR button board

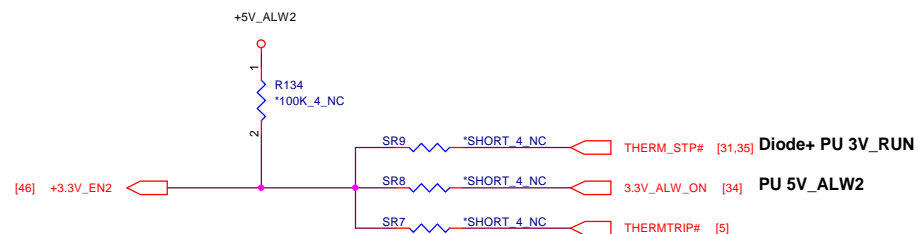
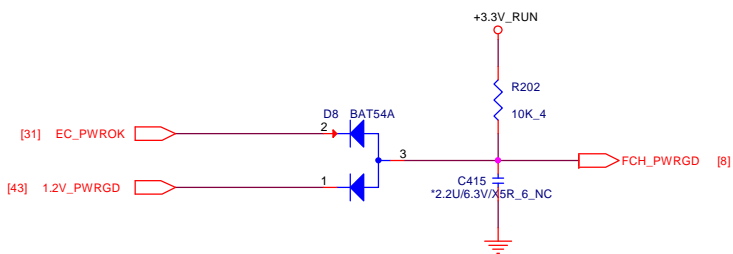




SYS_SHDN#	4.7K	6.8K	10K	15K	22K	33K
ALERT#	77 °C	83 °C	89 °C	95 °C	101 °C	107 °C
4.7K	77 °C	83 °C	89 °C	95 °C	101 °C	107 °C
6.8K	78 °C	84 °C	90 °C	96 °C	102 °C	108 °C
10K	79 °C	85 °C	91 °C	97 °C	103 °C	109 °C
15K	80 °C	86 °C	92 °C	98 °C	104 °C	110 °C
22K	81 °C	87 °C	93 °C	99 °C	105 °C	111 °C
33K	82 °C	88 °C	94 °C	100 °C	106 °C	112 °C



G781-1P8
SMBus address is 1001101xb (9Ah) (x is R/W bit).



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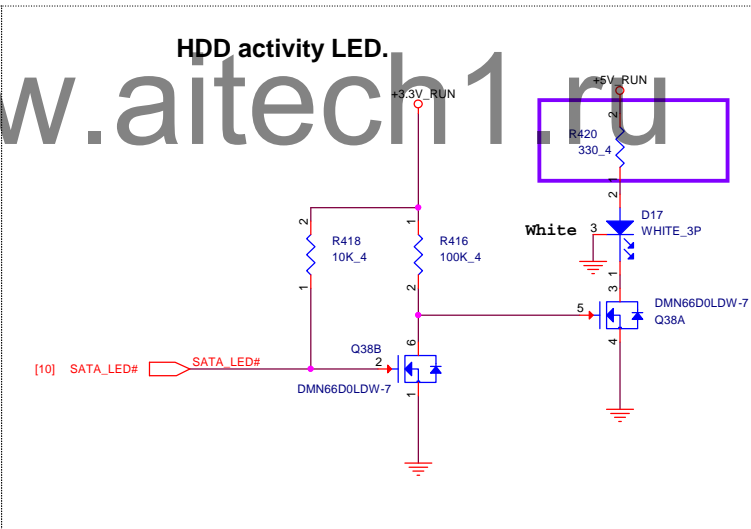
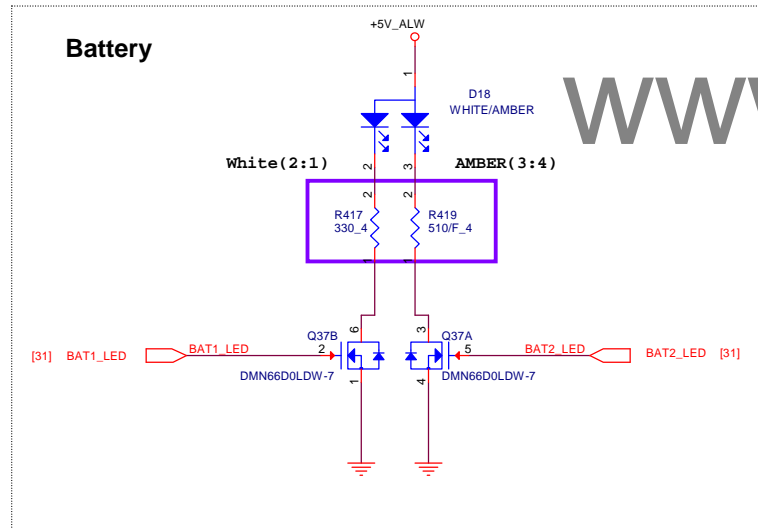
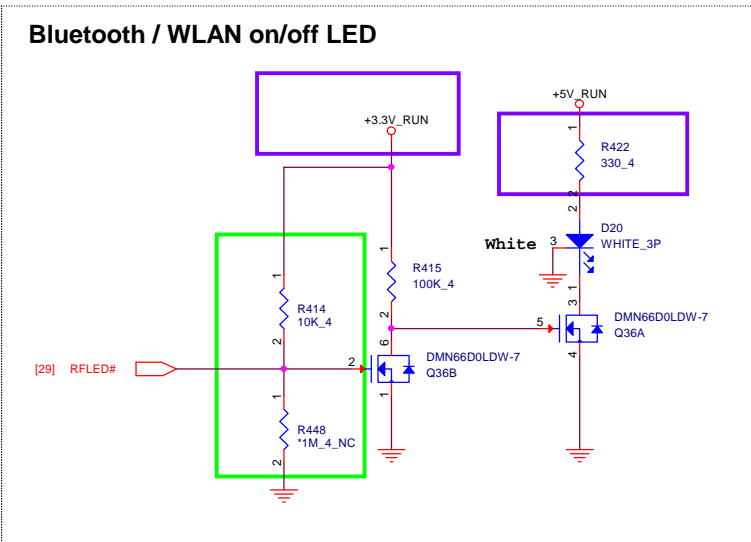
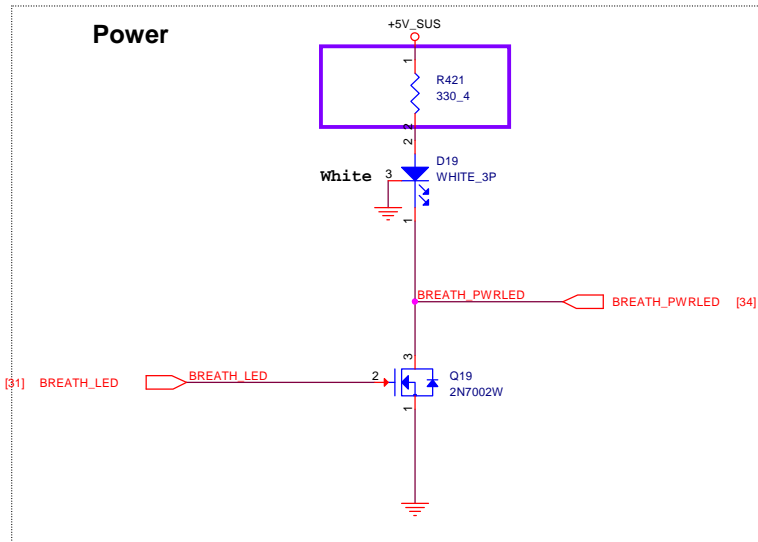


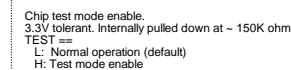
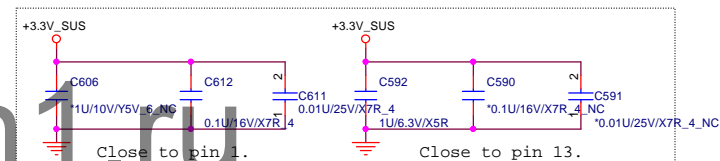
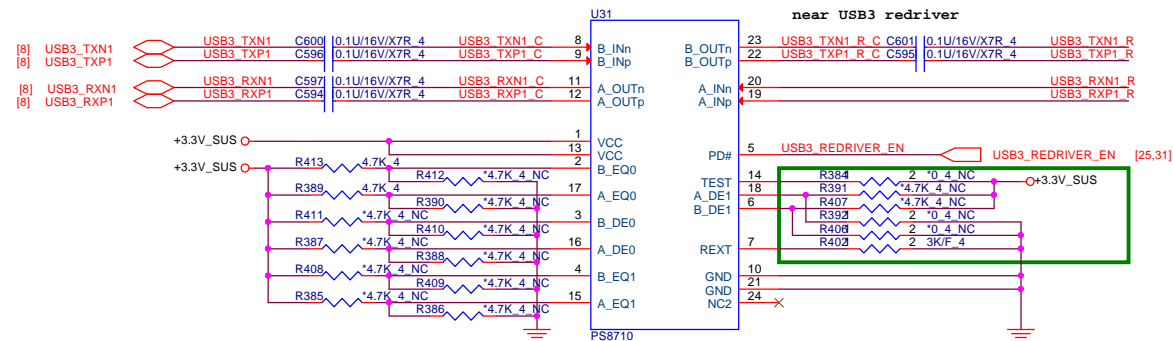
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System Reset Circuit





Programmable output pre-emphasis level setting for channel A
3.3V tolerant. Internally pulled down at ~ 150K ohm
[A_DE1, A_DE0] ==
LL: 3.5dB de-emphasis
LH: No de-emphasis
HH: 7dB de-emphasis with boost output swing
HL: 5dB de-emphasis with boost output swing

Equalizer control and program for channel A
3.3V tolerant. Internally pulled down at ~ 150K ohm
[A_EQ1, A_EQ0] ==
LL: adaptive EQ enable
LH: program EQ for channel loss up to 7dB
HL: program EQ for channel loss up to 14.5dB
HH: program EQ for channel loss up to 11.5dB

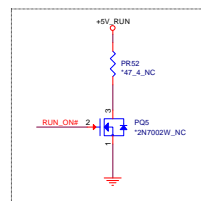
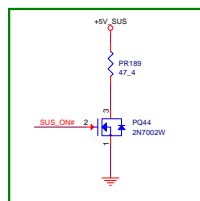
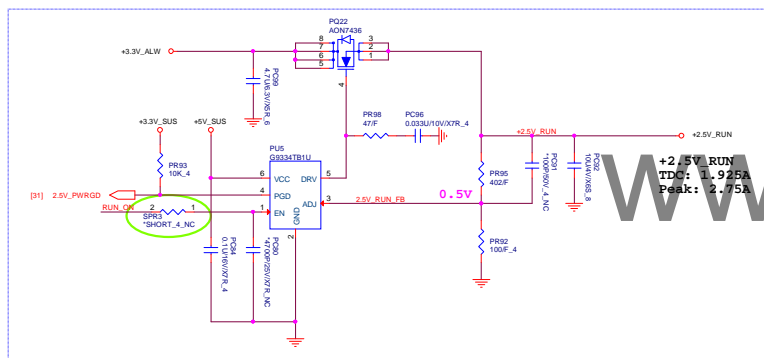
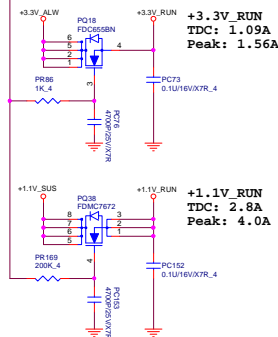
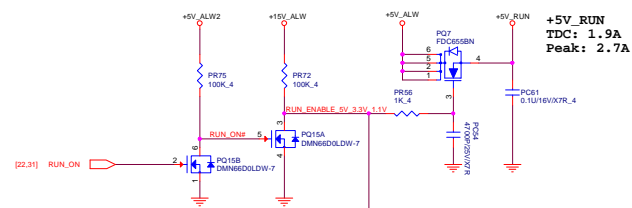
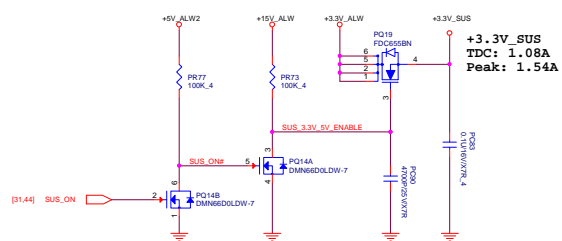
Programmable output pre-emphasis level setting for channel B
3.3V tolerant. Internally pulled down at ~ 150K ohm
[B_DE1, B_DE0] ==
LL: 3.5dB de-emphasis
LH: No de-emphasis
HL: 7dB de-emphasis with boost output swing
HH: 5dB de-emphasis with boost output swing

Equalizer control and program for channel B
3.3V tolerant. Internally pulled down at ~ 150K ohm
[B_EQ1, B_EQ0] =
LL: adaptive EQ enable
LH: program EQ for channel loss up to 7dB
HL: program EQ for channel loss up to 14.5dB
HH: program EQ for channel loss up to 11.5dB

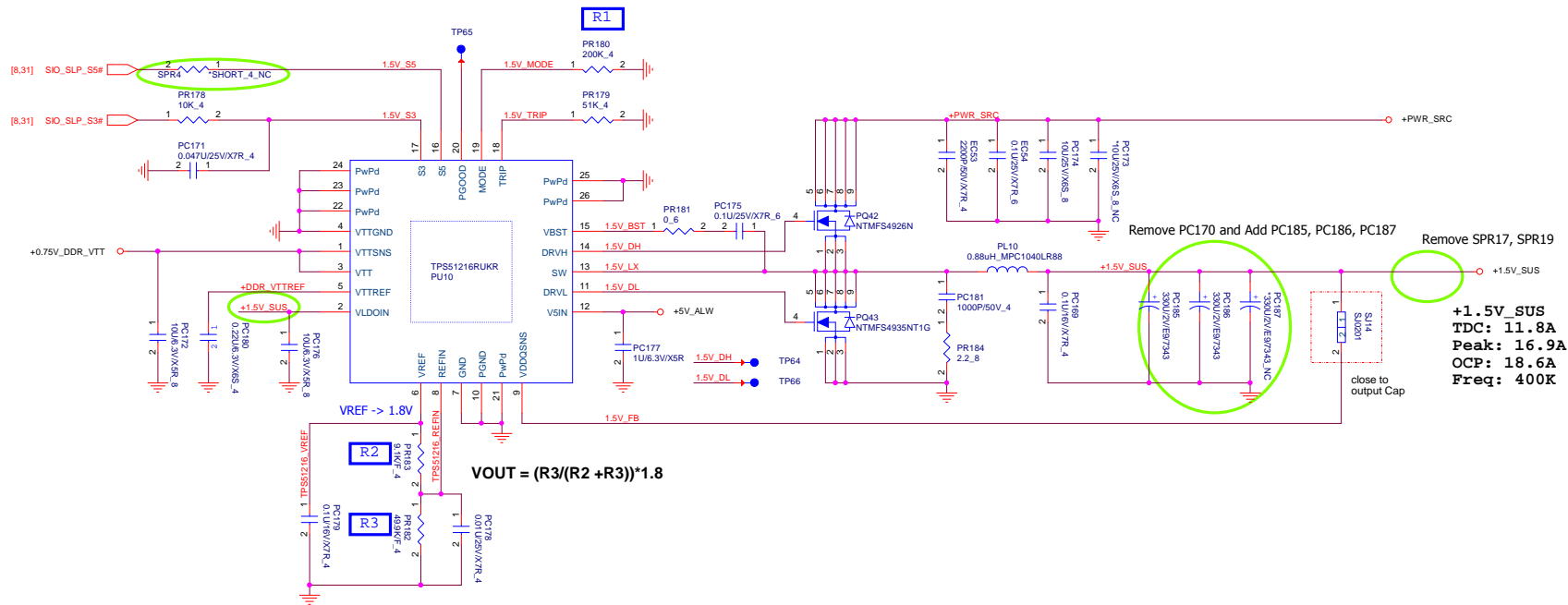
Adapter type	65W	90W
ADAPT_TRIP_SET	0	1
SETTING CURRENT	3.7A	5.6A

Register Address	Register Name
0x12H	ChargeOption()
0x14H	ChargeCurrent()
0x15H	ChargeVoltage()
0x3FH	InputCurrent()
0xFEH	ManufacturerID()
0xFFH	DeviceID()

<default>



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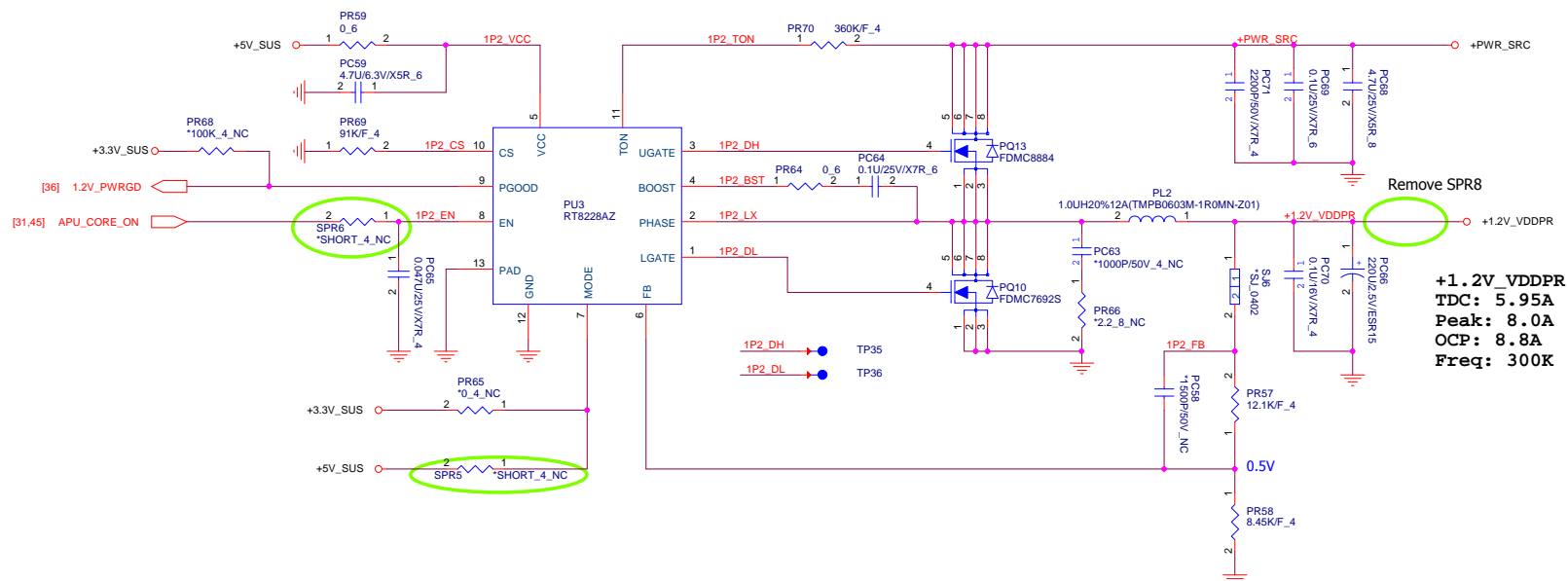
Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	Off (discharge)	Off (discharge)	Off (discharge)

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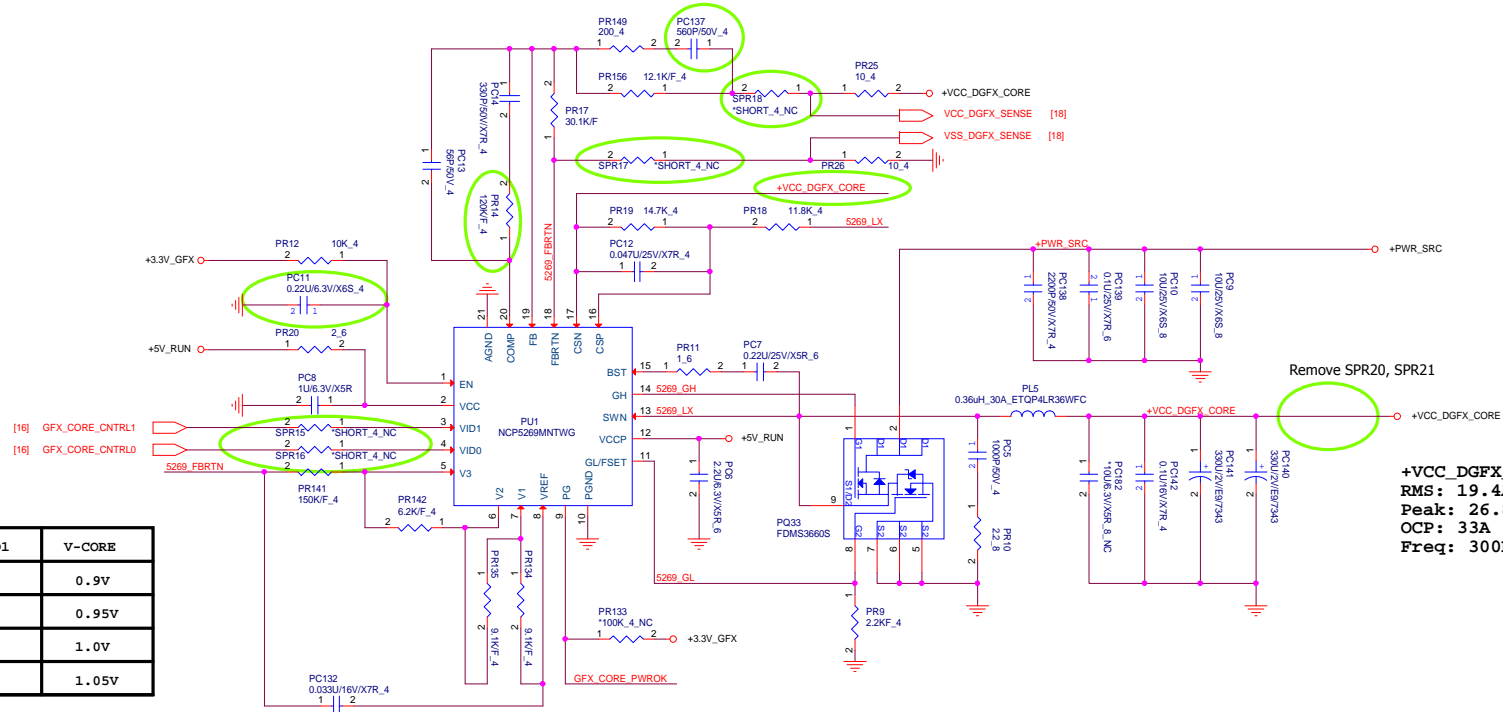
MODE Selection				
	Resistance between MODE and GND		Frequency	Discharge Mode
R1	200K_4	CS42002JB14	400k Hz	Tracking Discharge
R1	100K_4	CS41002JB20	300k Hz	
R1	68K_4	CS36802JB12	300k Hz	Non-tracking
R1	47K_4	CS34702JB21	400k Hz	Discharge

 Quanta Computer Inc. PROJECT : R0AA		Size	Document Number	Rev
			+1.5V_DDR/0.75V(TPS51216)	B
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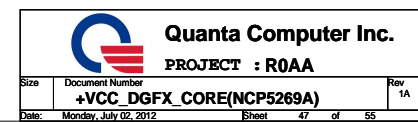


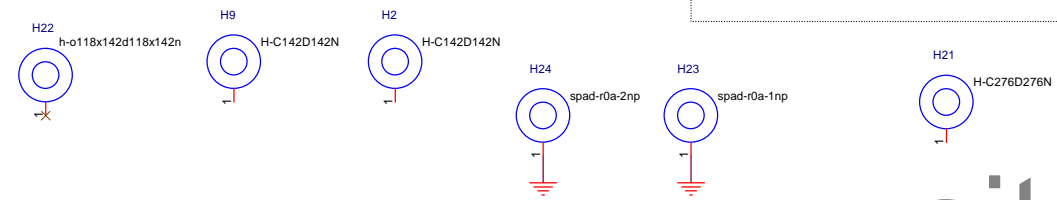
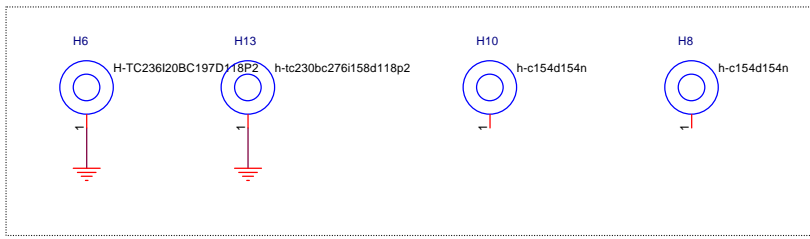
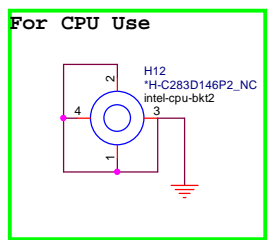
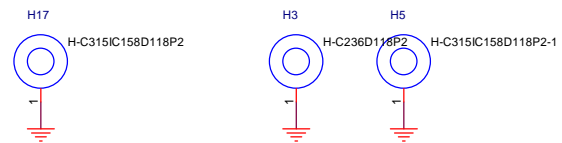
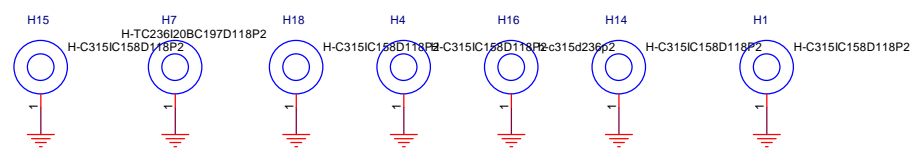
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